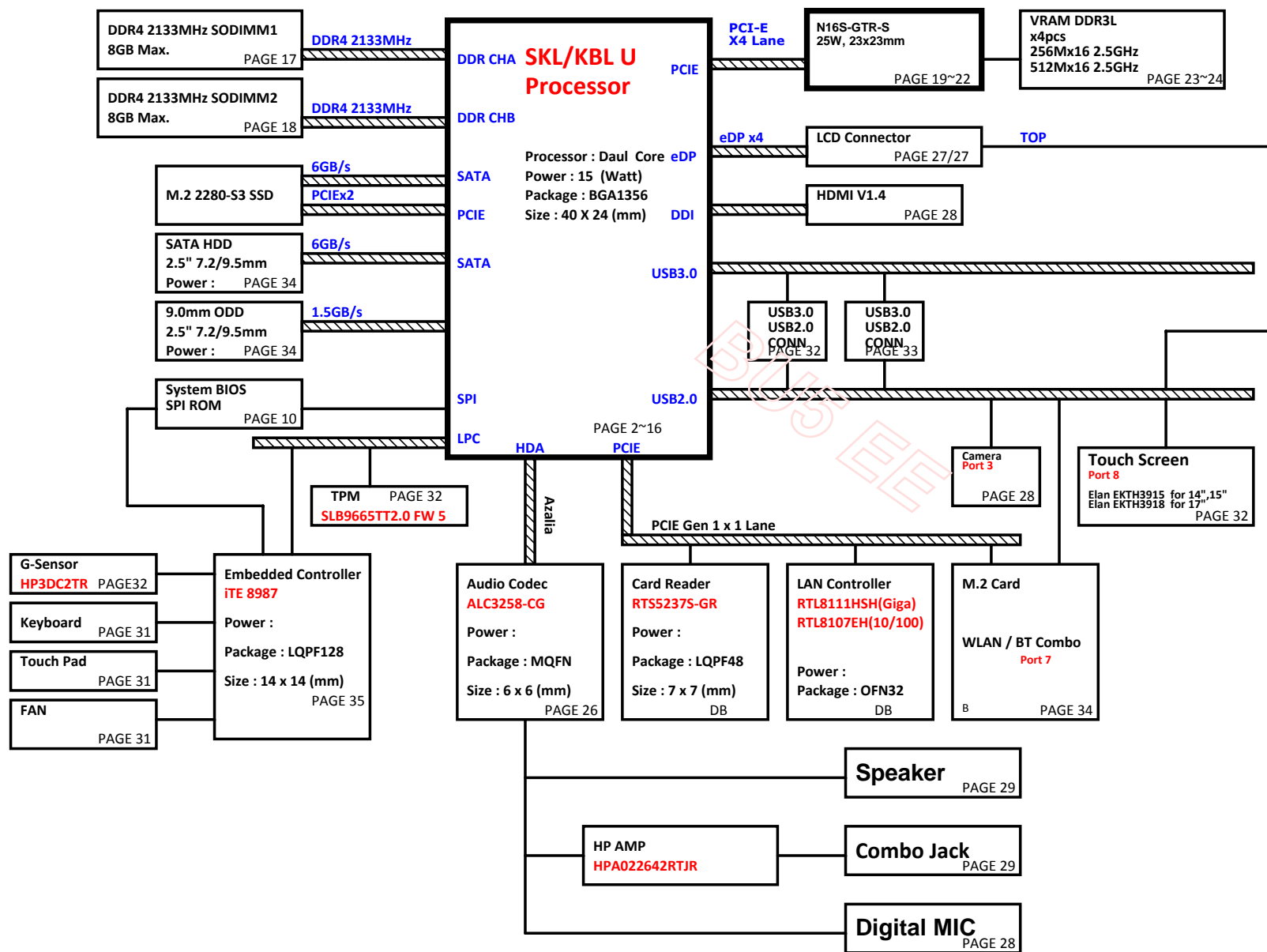


**LAYER 1 : TOP**  
**LAYER 2 : SGND**  
**LAYER 3 : IN1(High)**  
**LAYER 4 : IN2(Low)**  
**LAYER 5 : SVCC**  
**LAYER 6 : BOT**



+3V [4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,43,44,47]  
+1.0V [4,6,16,33,39]  
+VCCSTPLL [4,5,6,9,38,39]

## HDMI

[27] IN\_D2# IN\_D2# E55  
[27] IN\_D2 IN\_D2 F55  
[27] IN\_D1# IN\_D1# F58  
[27] IN\_D1 IN\_D1 F58  
[27] IN\_D0# IN\_D0# G53  
[27] IN\_D0 IN\_D0 F56  
[27] IN\_CLK# IN\_CLK# G56  
[27] IN\_CLK IN\_CLK G56

C50 DD12\_TXN[0] DDI  
C52 DD12\_TXP[0] DDI  
C52 DD12\_TXN[1] DDI  
C52 DD12\_TXP[1] DDI  
C52 DD12\_TXN[2] DDI  
C52 DD12\_TXP[2] DDI  
C52 DD12\_TXN[3] DDI  
C52 DD12\_TXP[3] DDI

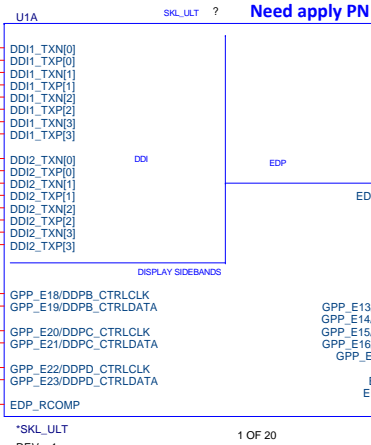
[27] SDVO\_CLK SDVO\_CLK L13  
[27] SDVO\_DATA SDVO\_DATA L12

TP2 DDPC\_CTRLDATA

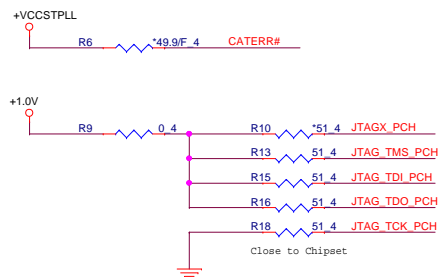
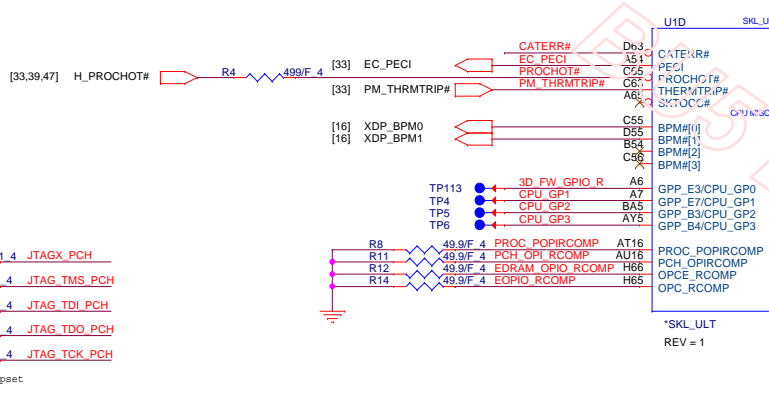
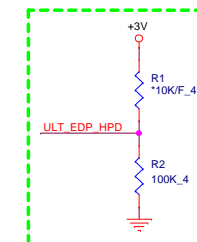
TP3 DDPC\_CTRLDATA

+VCCIO R3 24.9/F 4 EDP\_RCOMP E52

eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



Reserve EDP\_HPD opposites circuit!



Need apply PN

SKL\_ULT ?

JTAG

PROC\_TCK D61 XDP\_TCK0 [16]  
PROC\_TDI D60 XDP\_TDI\_CPU [16]  
PROC\_TDO A61 XDP\_TDO\_CPU [16]  
PROC\_TMS C60 XDP\_TMS\_CPU [16]  
PROC\_TRST# B59 XDP\_TRST#\_CPU [2,16]

B56 JTAG\_TCK\_PCH [16]  
D59 JTAG\_TDI\_PCH [16]  
A56 JTAG\_TDO\_PCH [16]  
C59 JTAG\_TMS\_PCH [16]  
C61 XDP\_TRST#\_CPU [2,16]  
A59 JTAGX\_PCH [16]

GPP\_E3/CPU\_GP0  
GPP\_E7/CPU\_GP1  
GPP\_B3/CPU\_GP2  
GPP\_B4/CPU\_GP3

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP

PROC\_TCK  
PROC\_TDI  
PROC\_TDO  
PROC\_TMS  
PROC\_TRST#

PCH\_JTAG\_TCK  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TDO  
PCH\_JTAG\_TMS  
PCH\_TRST#

JTAGX

PROC\_POPIRCOMP  
PCH\_POPIRCOMP  
OPCE\_RCOMP  
OPC\_RCOMP



Need apply PN



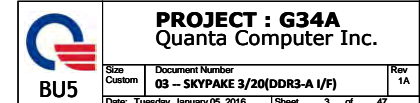
\*SKL\_ULT

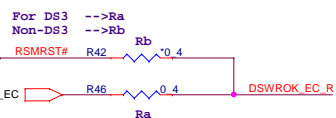
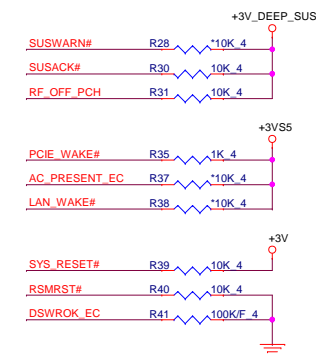
2 OF 20



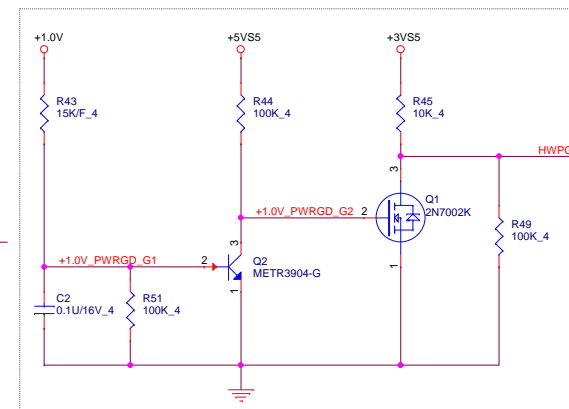
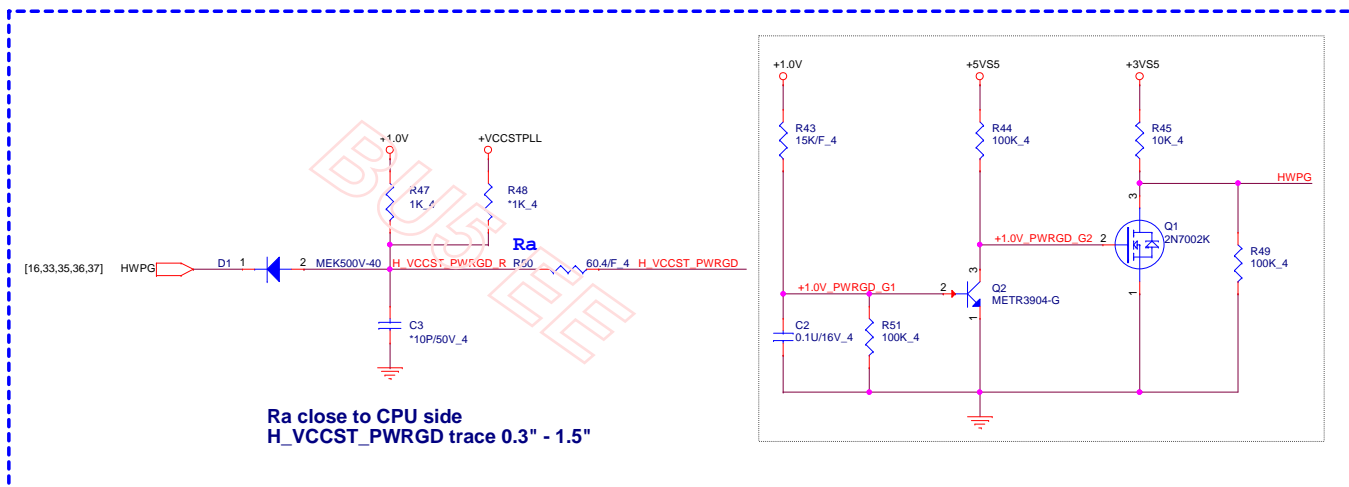
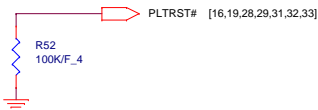
\*SKL\_UL

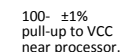
3 OF 20



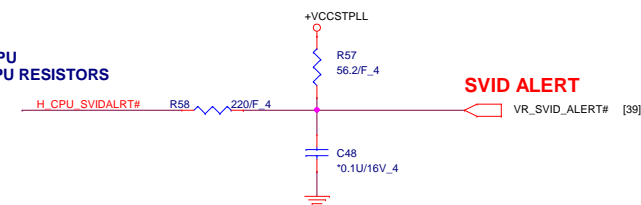


Check Rise/Fall time less than 100ns

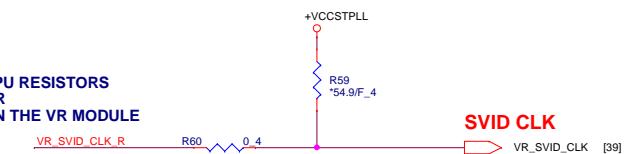




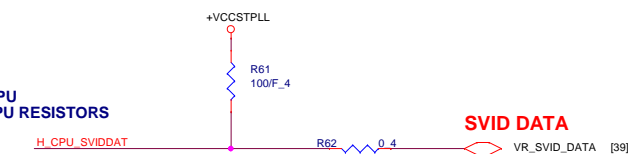
**CLOSE TO CPU  
PLACE THE PU RESISTORS**



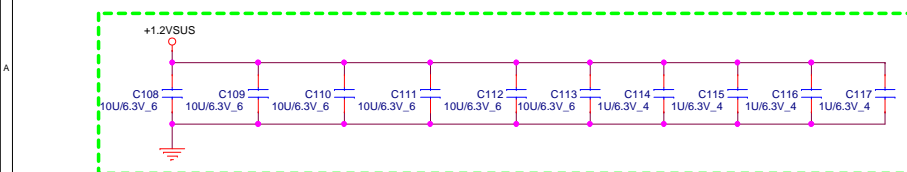
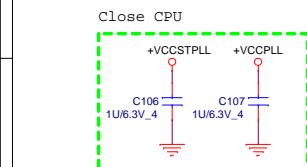
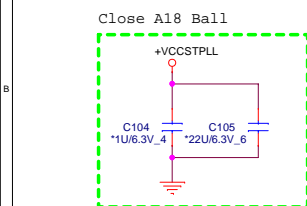
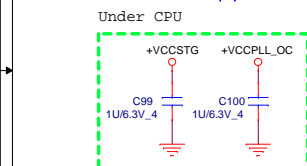
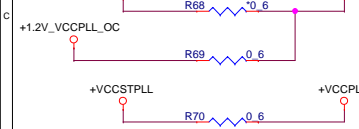
PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE



**CLOSE TO CPU  
PLACE THE PU RESISTORS**

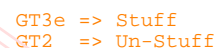



Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTX</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

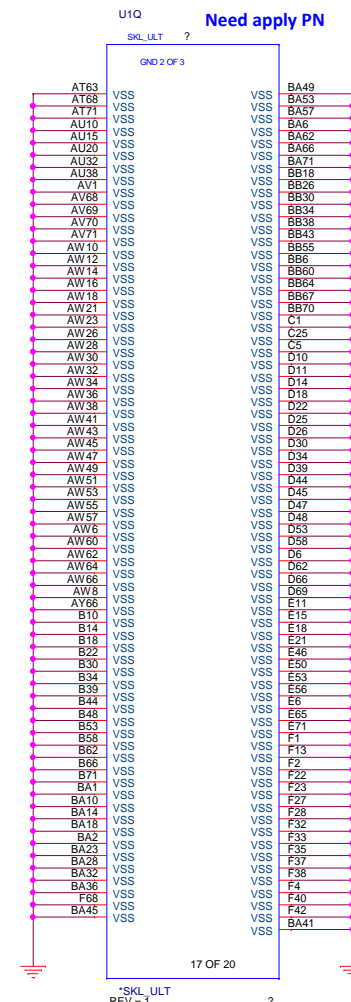
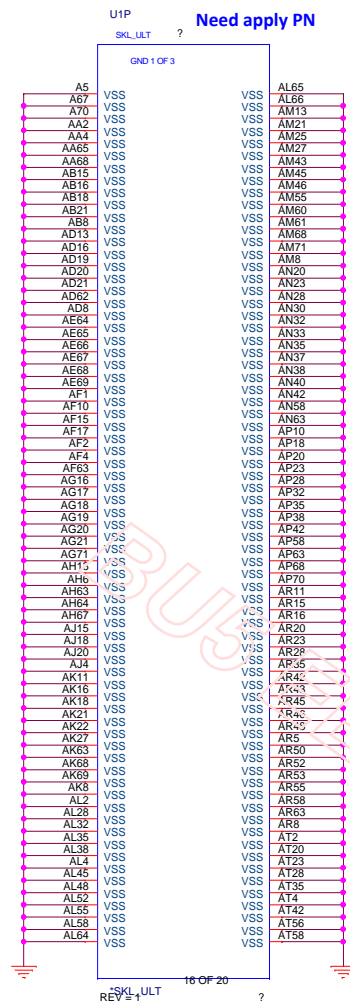
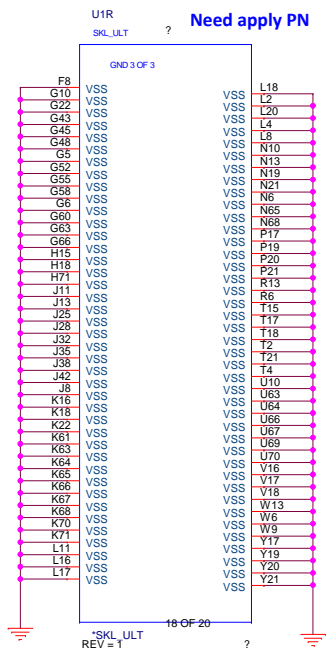


Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CC_GT</sub>	Processor Graphics Power Rails	SVID
V <sub>CC_GTX</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CC_SA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CC_IO</sub>	IO Power Rail	Fixed
V <sub>CC_ST</sub>	Sustain Power Rail	Fixed
V <sub>CC_PLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CC_OPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CC_OPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CC_EOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

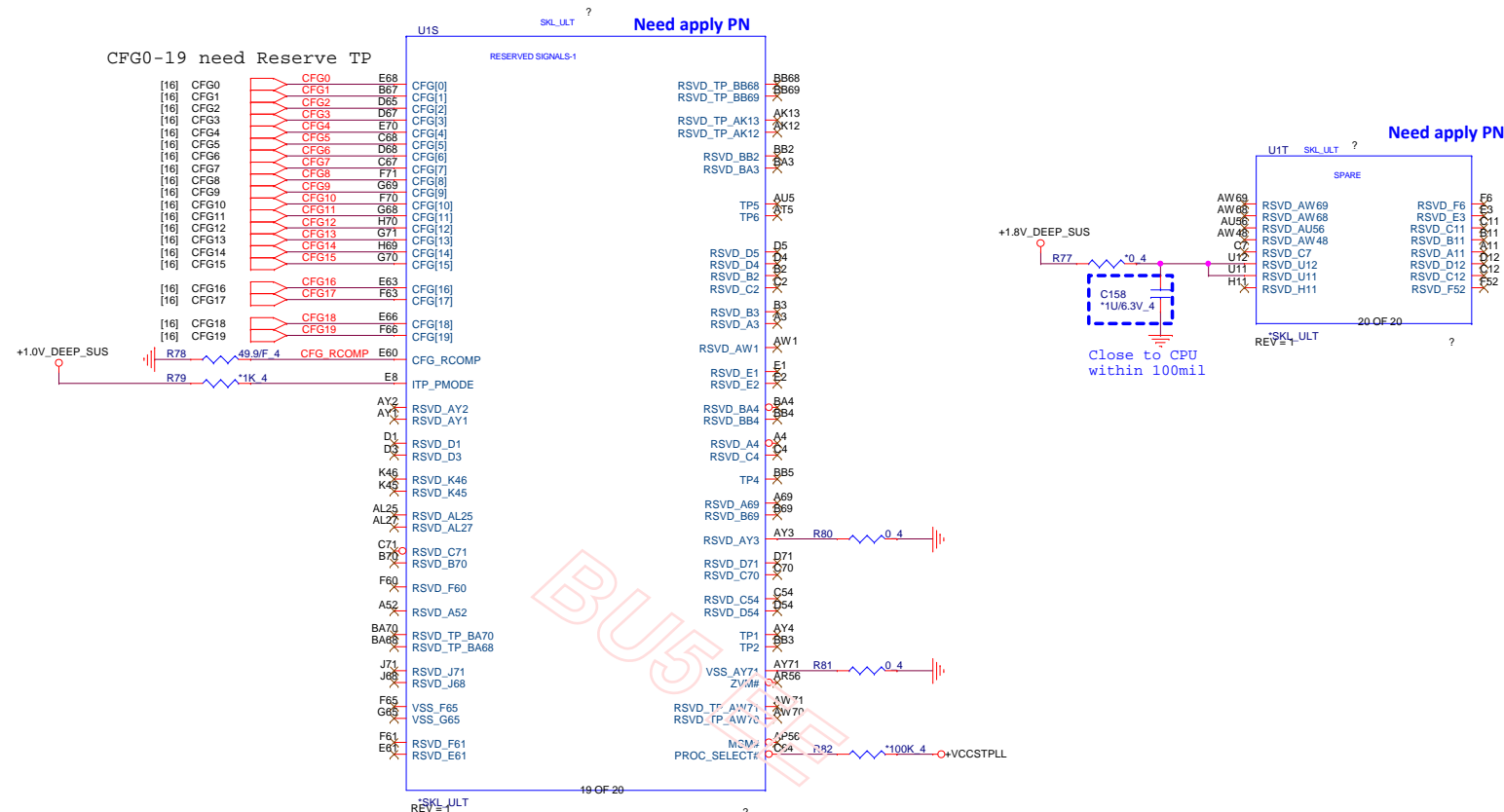




 <b>BU5</b>	<b>PROJECT : G34A</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>07 -- SKYPAKE 8/20 (POWER-3)</b>	Rev 1A
	Date: Tuesday, January 05, 2016	Sheet 7 of 47	







**Processor Strapping** The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 ~1K 4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 ~1K 4



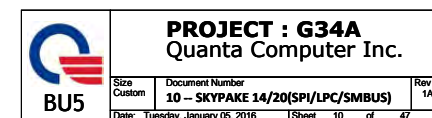
[33]	PCH_SPI_CS0#_R		PCH_SPI_CS0#_R
[33]	PCH_SPI1_CLK_R		PCH_SPI1_CLK_R
[33]	PCH_SPI1_SI_R		PCH_SPI1_SI_R
[33]	PCH_SPI1_SO_R		PCH_SPI1_SO_R

TP17	PCH SPI CS0# R
TP18	PCH SPI1 CLK R
TP19	PCH SPI1 SI R
TP20	PCH SPI1 SO R
TP21	BIOS WP#
TP22	HOLD#

### PCH SPI ROM(CLG)

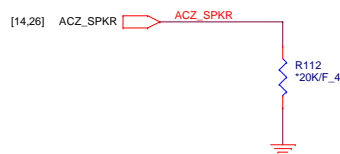


### SMBus/Pull-up(CLG)

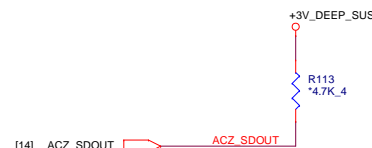


# Functional Strap Definitions

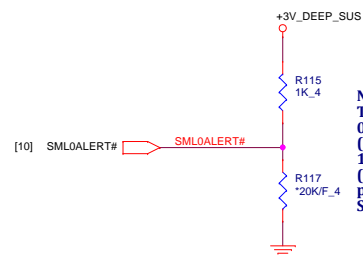
**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET



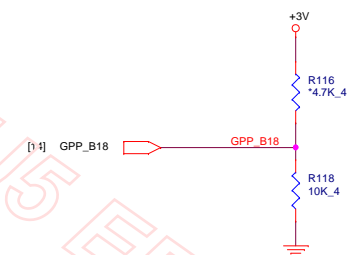
**TOP SWAP OVERRIDE**  
HIGH - TOP SWAP ENABLE  
LOW-DISABLED  
HIGH: LPC SELECTED FOR SYSTEM FLASH  
WEAK INTERNAL PD



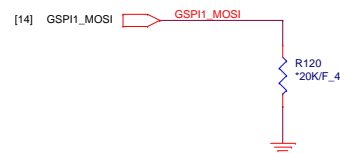
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



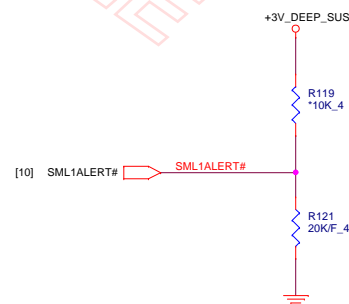
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).  
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable No Reboot mode.  
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



**No Boot:**  
The signal has a weak internal pull-down.  
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.  
Bit 10 Boot BIOS Destination  
0 SPI  
1 LPC

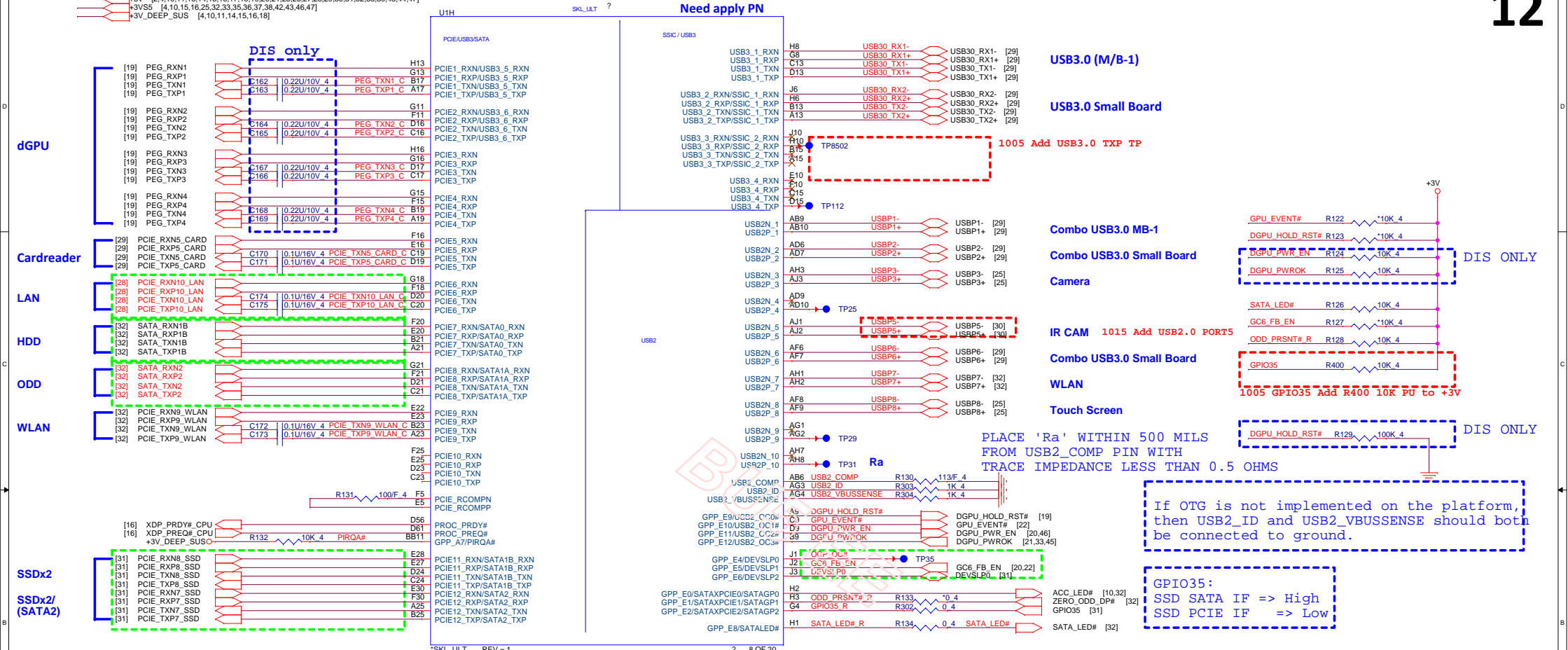


**No Boot:**  
The signal has a weak internal pull-down.  
0 = LPC is selected for EC.  
1 = eSPI is selected for EC.


 +3V [2,4,10,11,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,43,44,47]  

 +3VS5 [4,10,15,16,25,32,33,35,36,37,38,42,43,46,47]  

 +3V\_DEEP\_SUS [4,10,11,14,15,16,18]



## PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	CR
Port3	dGPU	Port2	SSD
Port4	dGPU	Port3	WLAN
Port5	CardReader	Port4	LAN
Port6	LAN	Port5	Un-used
Port7	HDD		
Port8	ODD		
Port9	WLAN		
Port10	Un-used		
Port11	SSDx2		
Port12	SSDx2/ SATA2		

### USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	Cobime USB3.0 Small Board
PORT-3	NC
PORT-4	NC

```
1005 Change Name from DEVSLP2 to DEVSLP0
DEVSLP0 and GC6_FB_EN SWAP
1005 GPIO35 and ACC_LED# SWAP
```

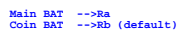
## USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 Small Board
PORT-3	Camera
PORT-4	NC
PORT-5	IR CAM
PORT-6	Cobime USB3.0 Small Board
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC



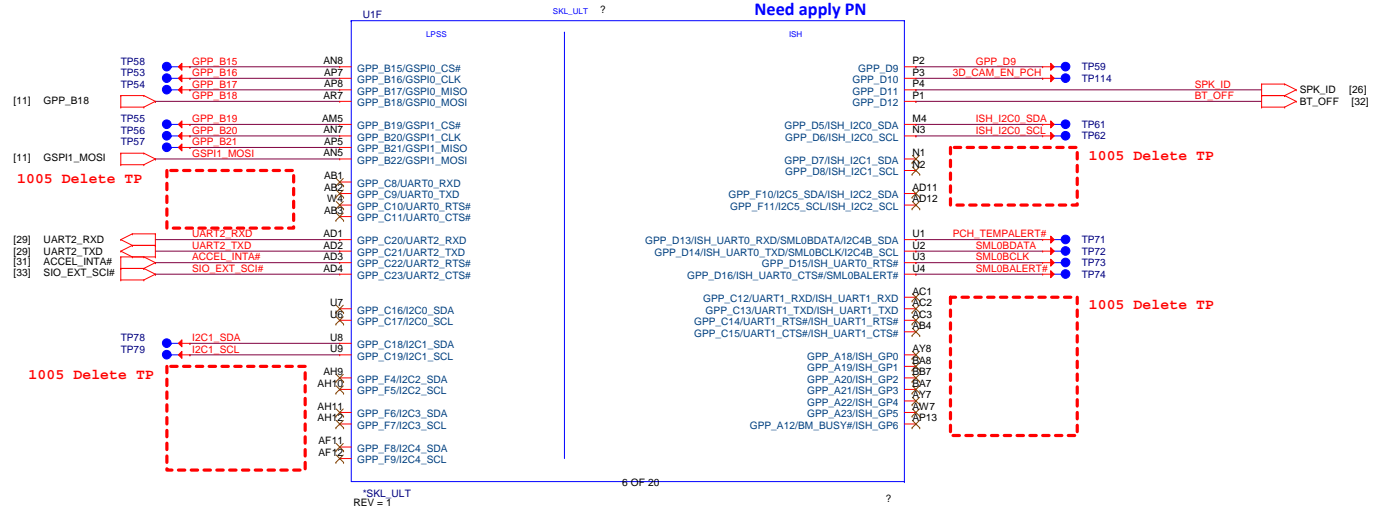
Sumins

Pin	Signal	Change
+3V_RTC_2	+BAT_RTC	1005 Change +3V_RTC to +BAT_RTC



The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.





3+V\_DEEP\_SUS

[26] ACZ\_SYNC\_AUDIO

[26] ACZ\_RST#\_AUDIO

[25] ACZ\_SDOUT\_AUDIO

[26] BIT\_CLK\_AUDIO

R160

R161

R165

R168

1K 4

33 4

33 4

33 4

33 4

C183

15750V 4

ACZ\_SYNC

ACZ\_SYNC\_AUDIO

ACZ\_RST#

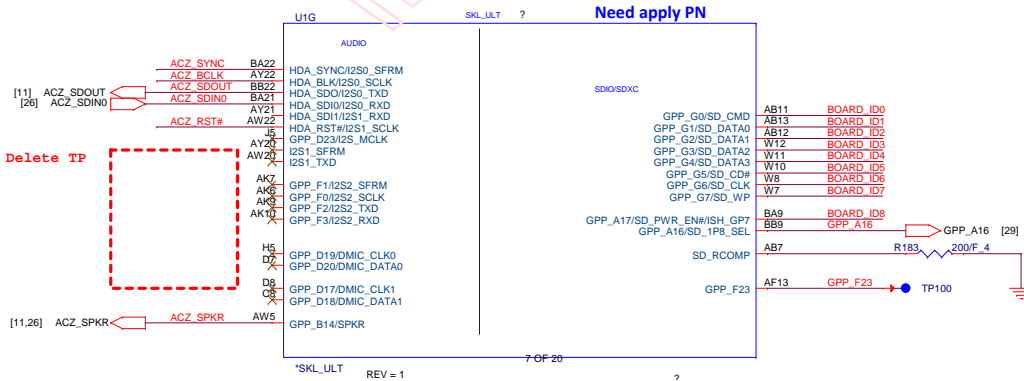
ACZ\_RST#\_AUDIO

ACZ\_SDOUT

ACZ\_SDOUT\_AUDIO

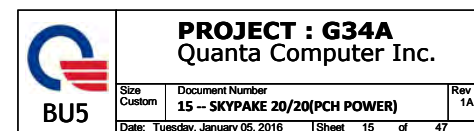
ACZ\_BCLK

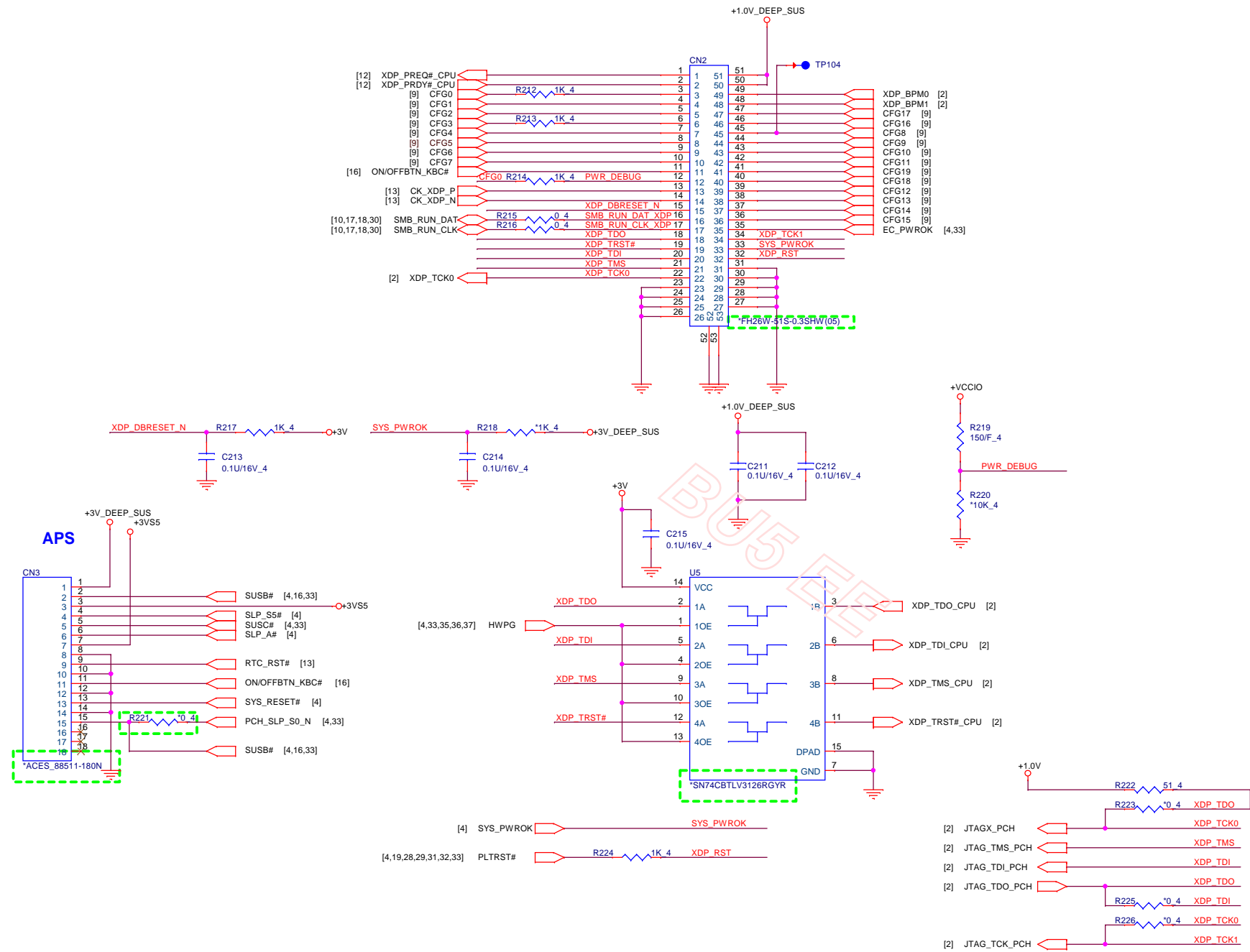
BIT\_CLK\_AUDIO

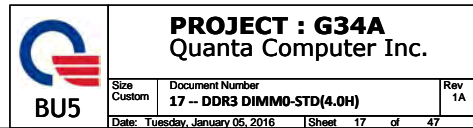


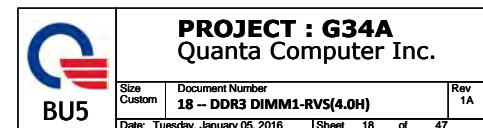
Skylake <sub>v</sub>	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6 ID5	ID4 ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	Reserve (Default = 00)	00 14" 01 15" 10 Reserve 11 Reserve	0 : UMA 1 : DIS

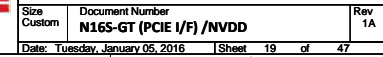


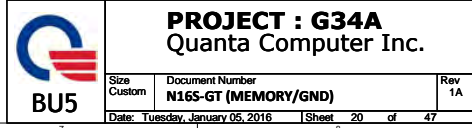




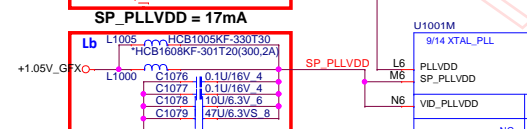
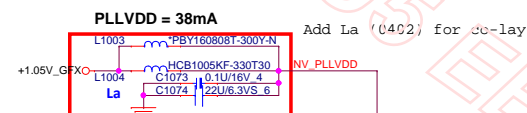
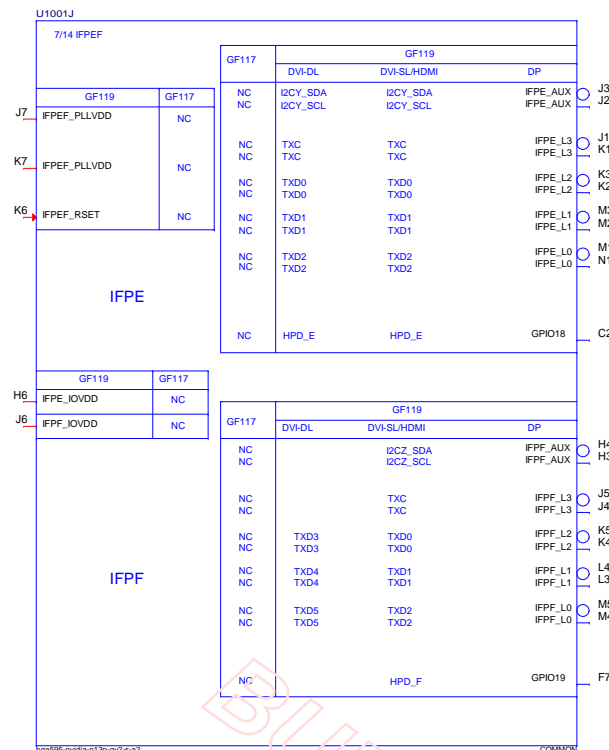
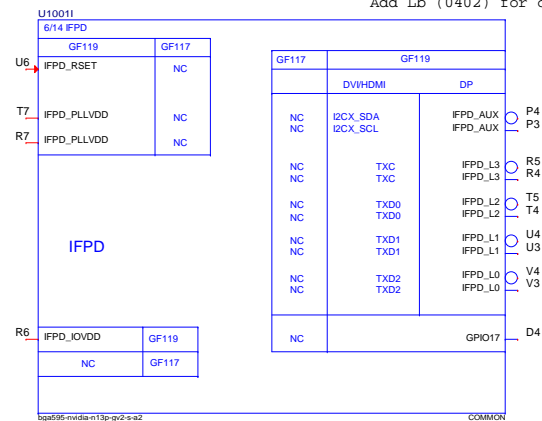
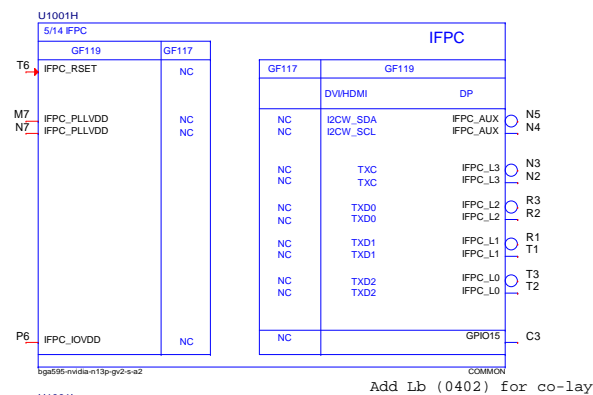
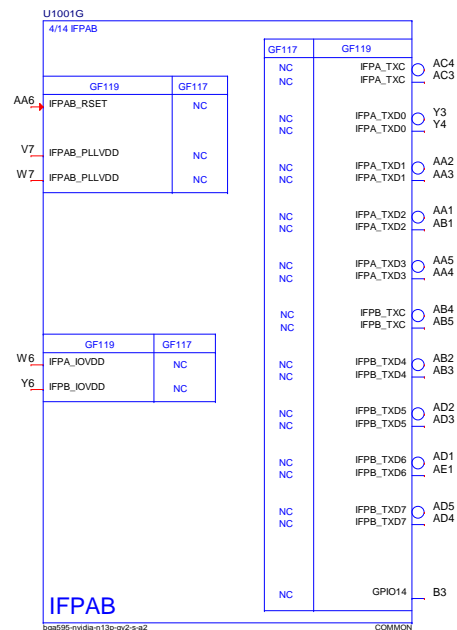




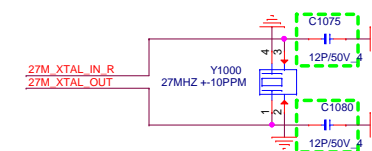
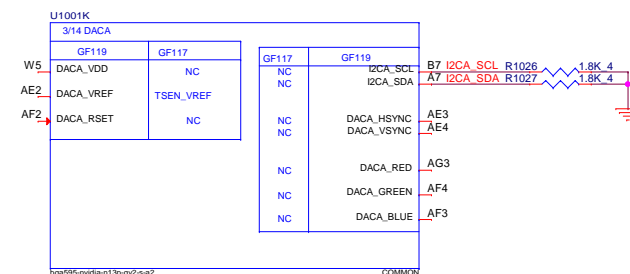
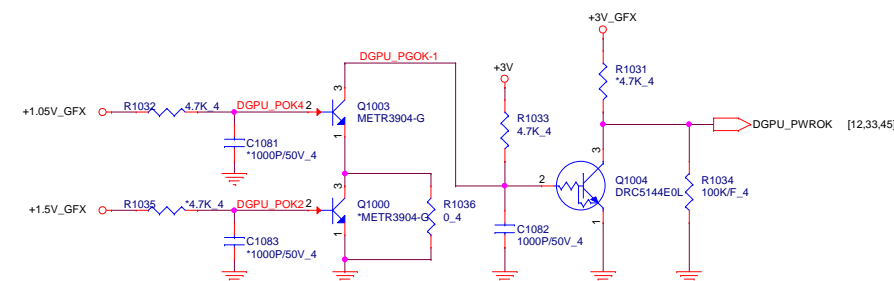


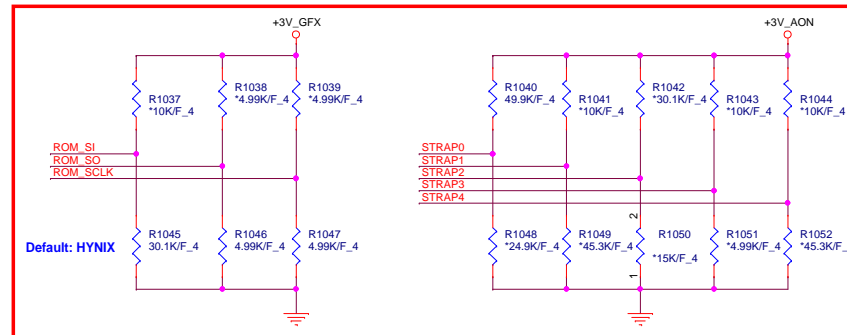




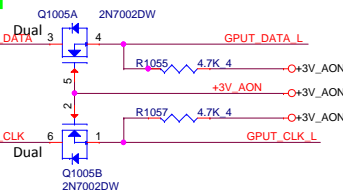


**VID\_PLLVDD = 41mA**



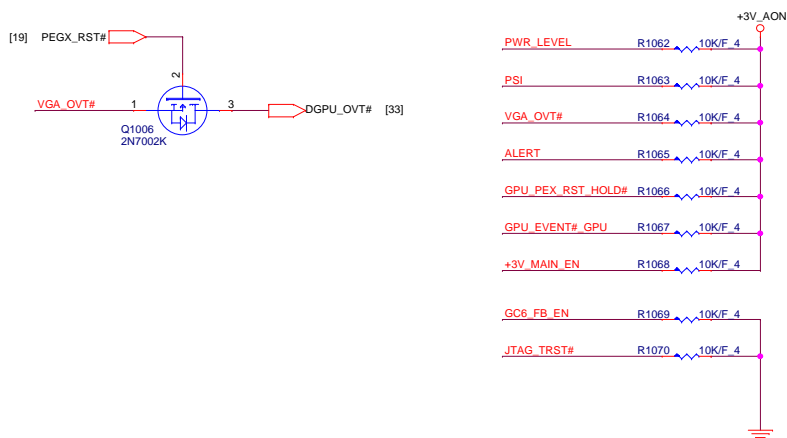


Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



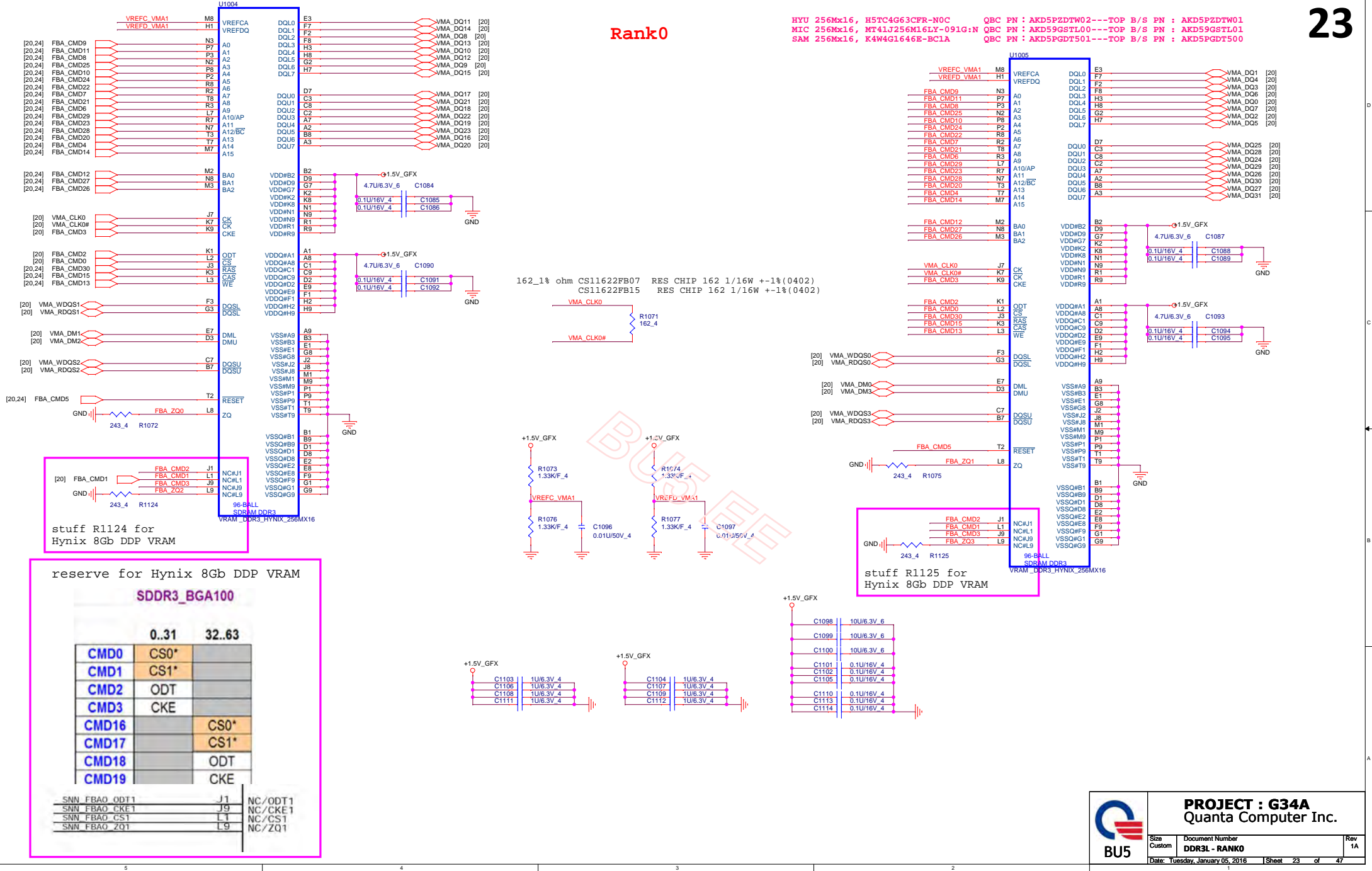
RAM CFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	Strapping	TOP B/S	QBC
0001	DDR3 256Mx16, 64bit, 2Gb,900MHz	Micron	MT41J7256M16LY-091G:N	0x3	AKD59GSTL01	AKD59GSTL00
0100	DDR3 256Mx16, 64bit, 2Gb,900MHz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PQDT500	AKD5PQDT501
1000	DDR3 256Mx16, 64bit, 2Gb,900MHz	HYNIX	H5TC4G63CFR-NOC	0x5	AKD5PZDTW01	AKD5PZDTW02
1001	DDR3 512Mx16, 64bit, 4Gb,900MHz	Micron	MT41K512M16HA-107G:A	0x9	AKD5QSGSTL05	AKD5QSGSTL09
1111	DDR3 512Mx16, 64bit, 4Gb,900MHz	HYNIX	H5TC8G63CMR-11C	0x9	AKD5QFDTW00	AKD5QFDTW01

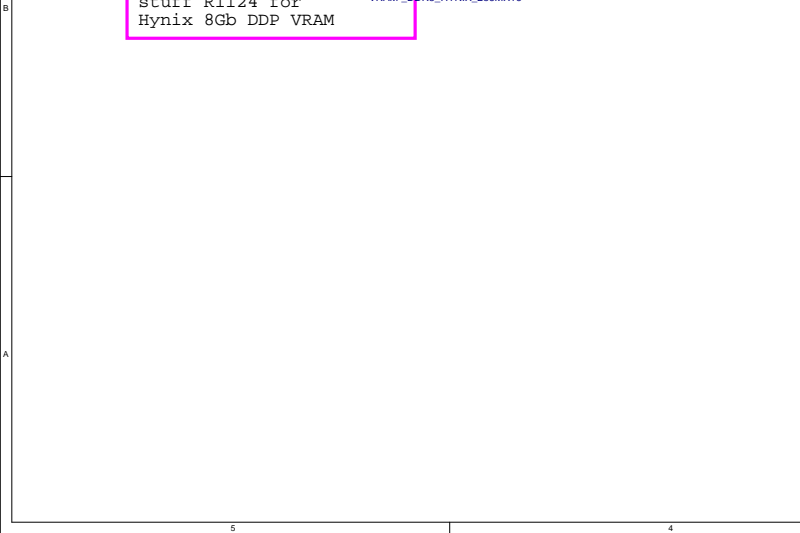
GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D_VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



Rank0

HYU 256Mx16, H5TC4G63CFR-N0C QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01  
MIC 256Mx16, MT41J256M16LY-091G-N QBC PN : AKD59GSTL00---TOP B/S PN : AKD59GSTL01  
SAM 256Mx16, K4W4G1646E-BC1A QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500

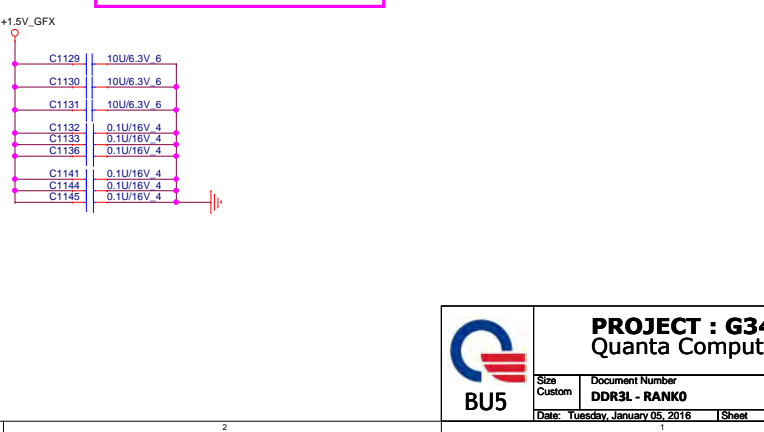
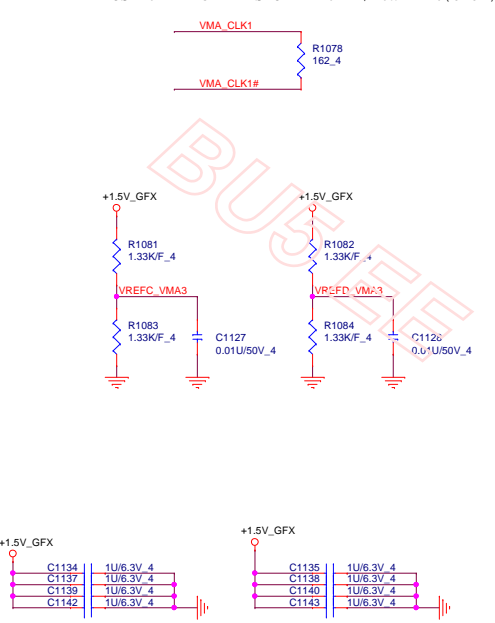




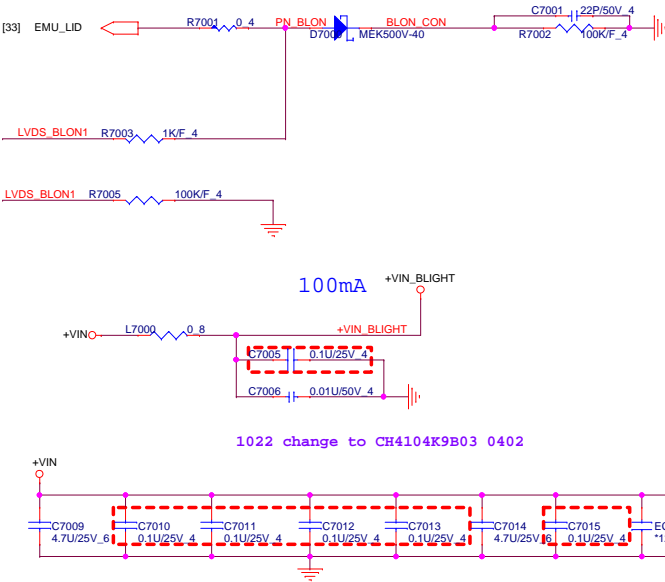
```

HYU 256Mx16, H5TC4G63CFR-N0C      QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01
MIC 256Mx16, MT41J256M16LY-091G:N  QBC PN : AKD59GSTL00---TOP B/S PN : AKD59GSTL01
SAM 256Mx16, K4W4G1646E-BC1A       QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500

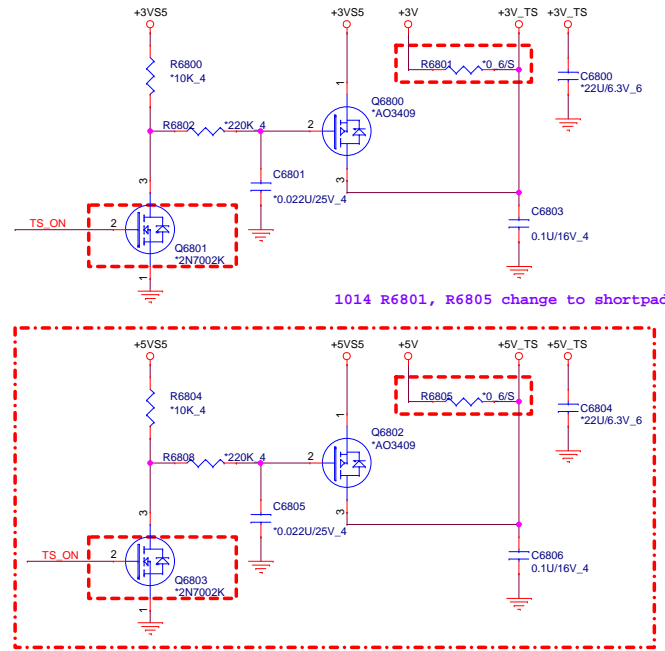
```



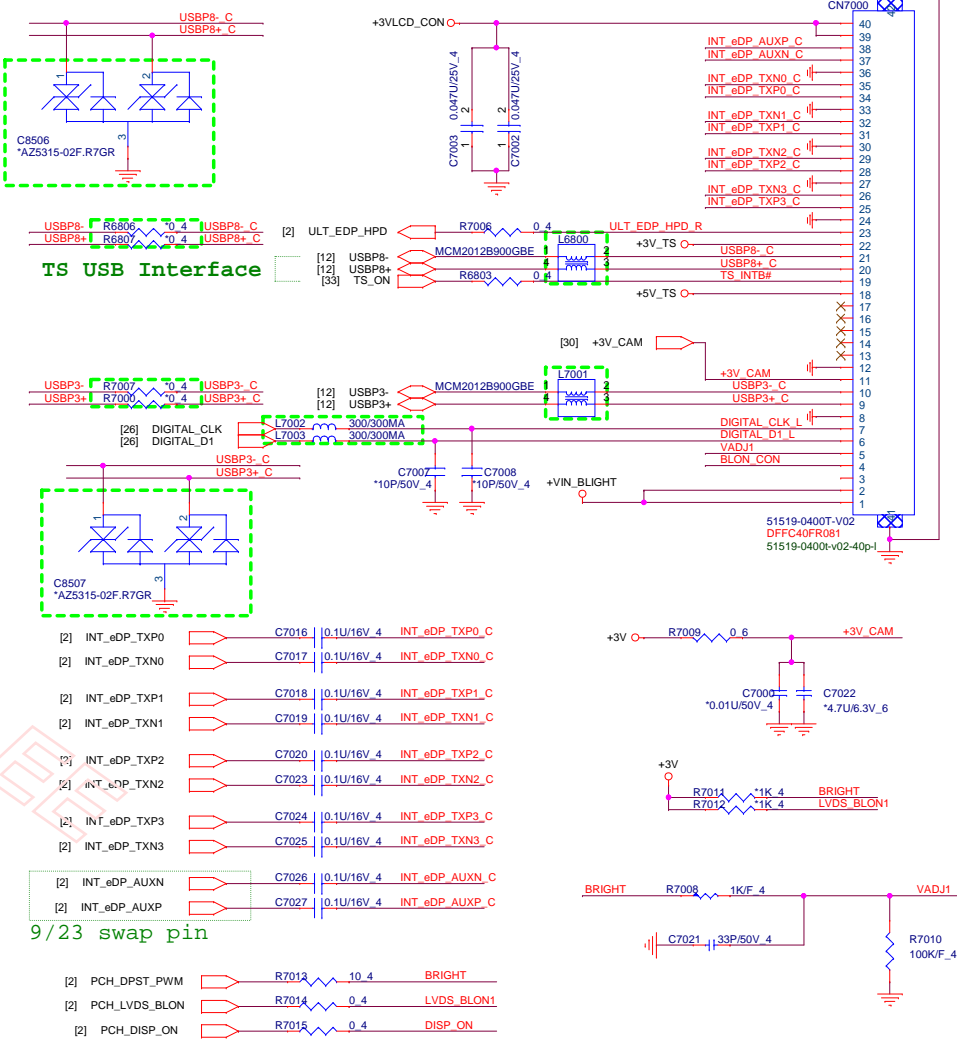
LID Switch



Touch screen

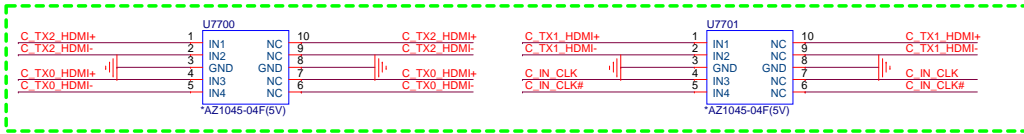
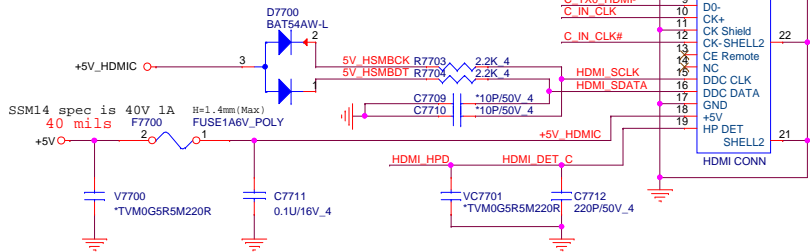
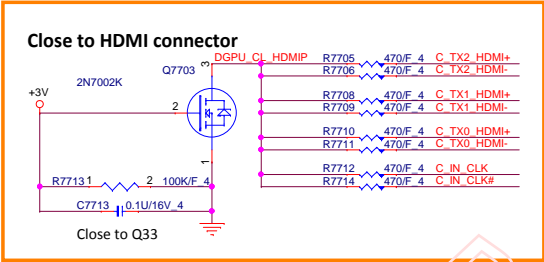
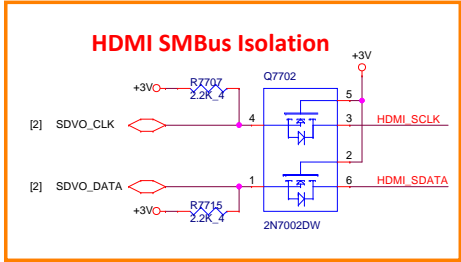
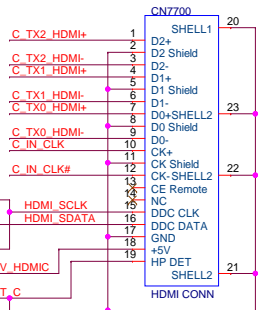
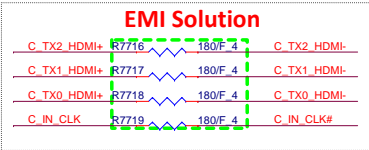
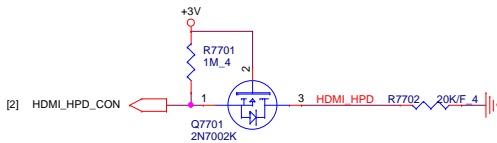
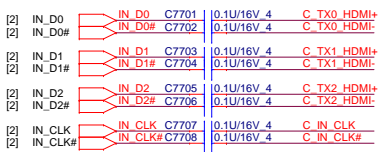


eDP Conn.

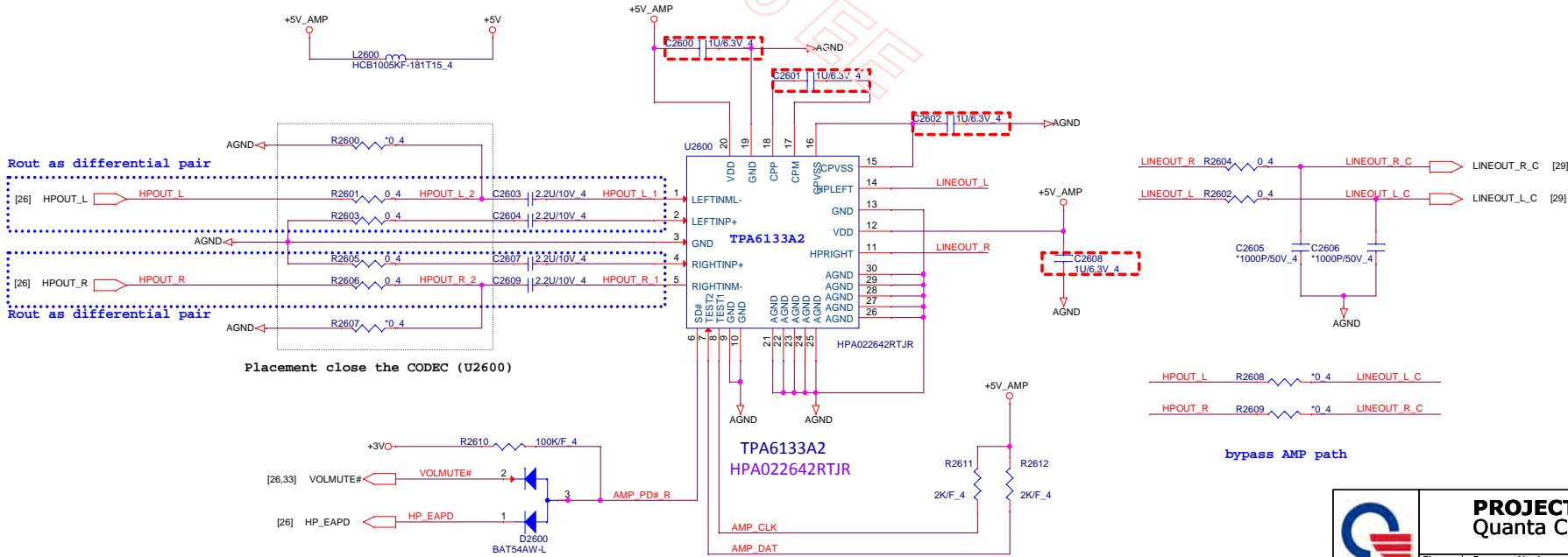


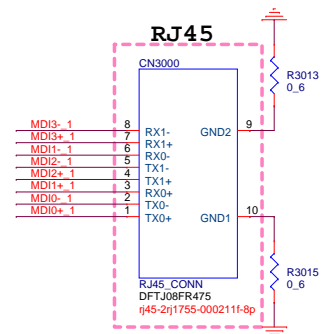
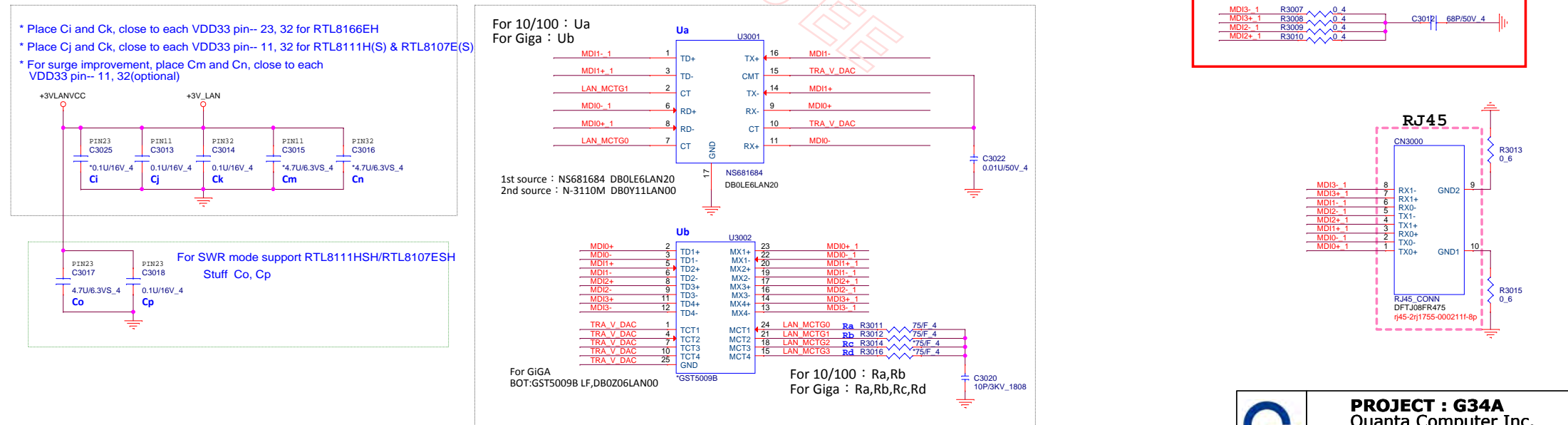




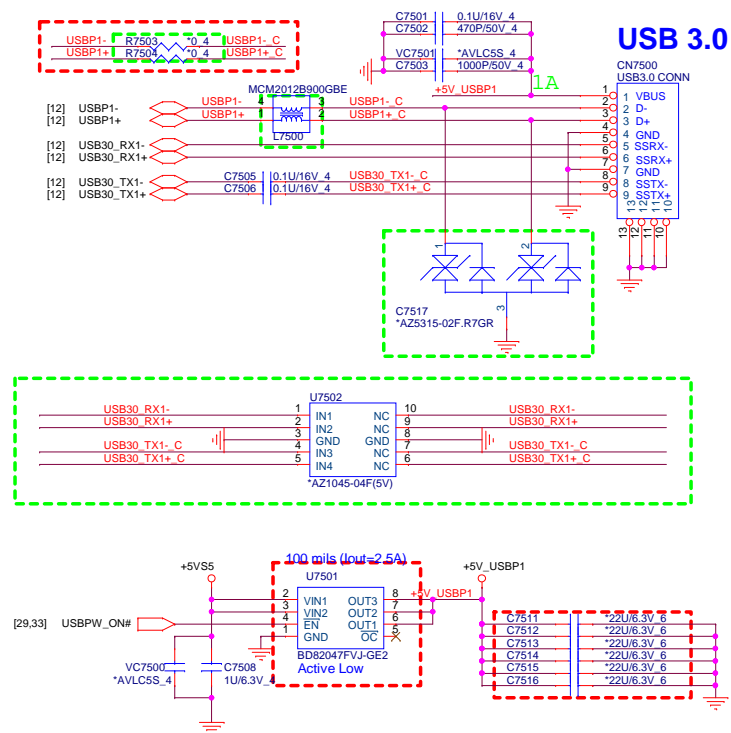


Head Phone out

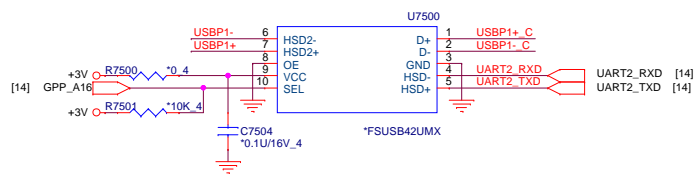




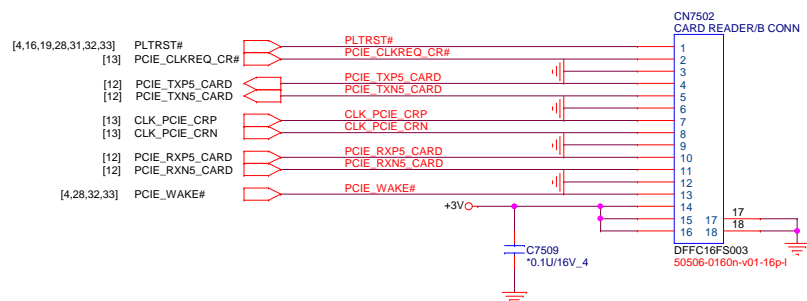
## USB 2.0/3.0 Combo



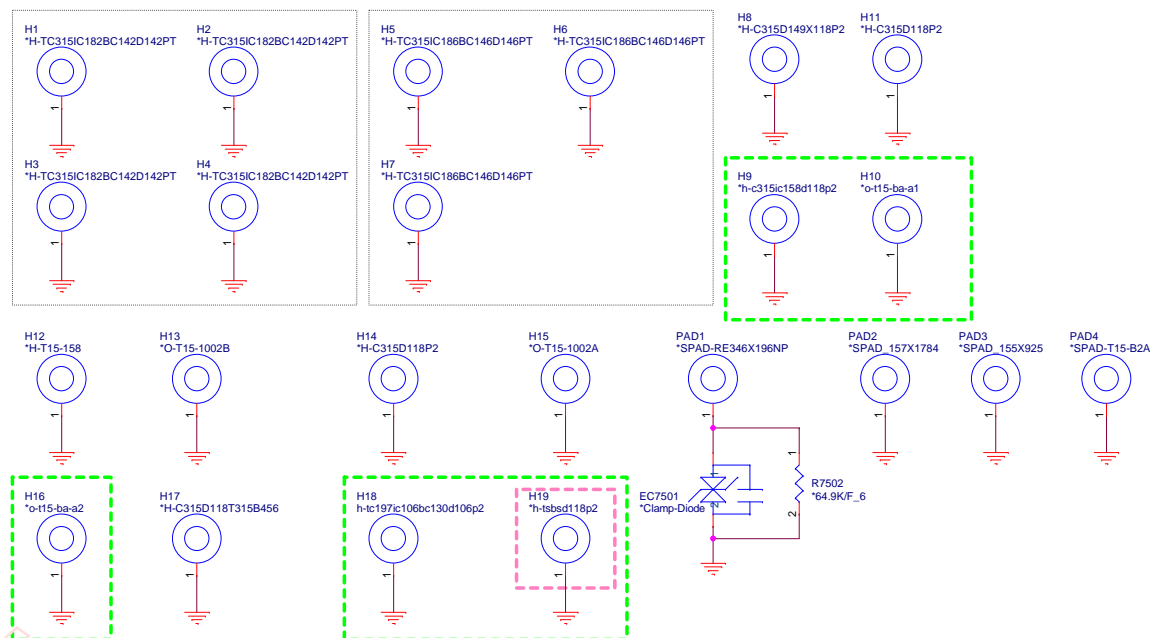
## UART for DEBUG



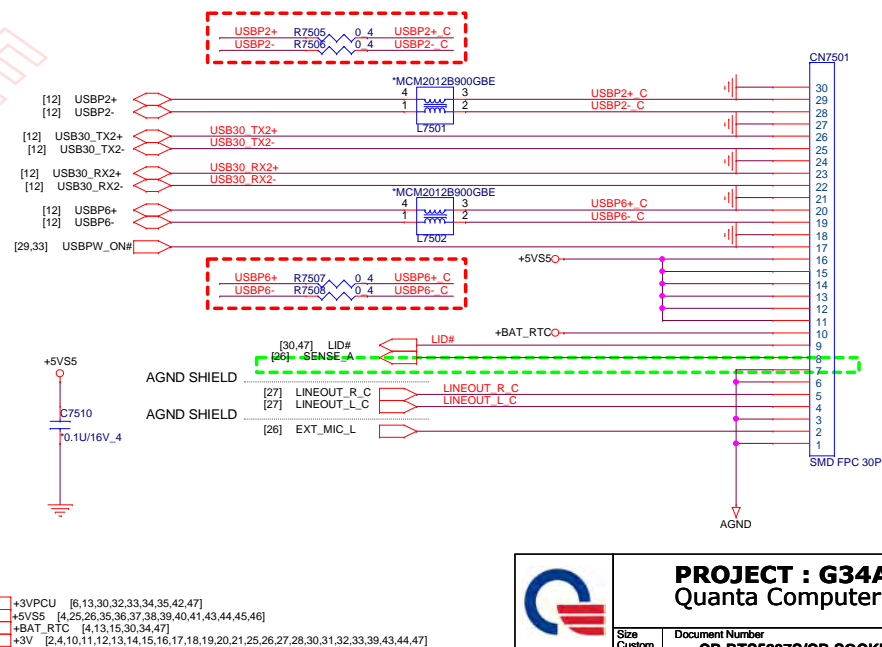
## Card Reader Connector

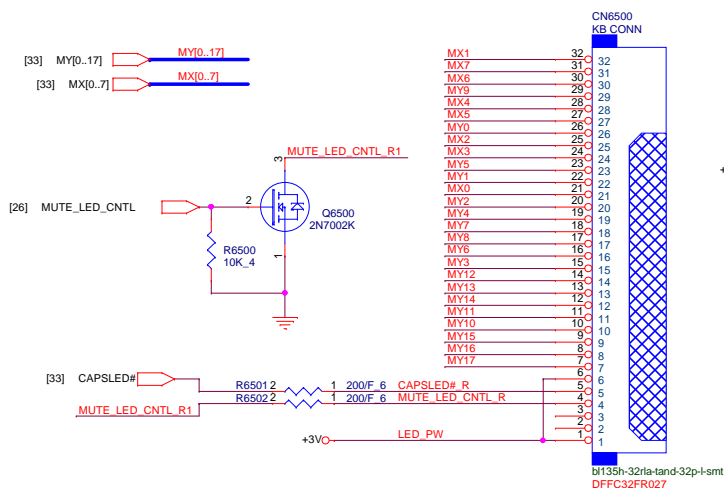


## Holes

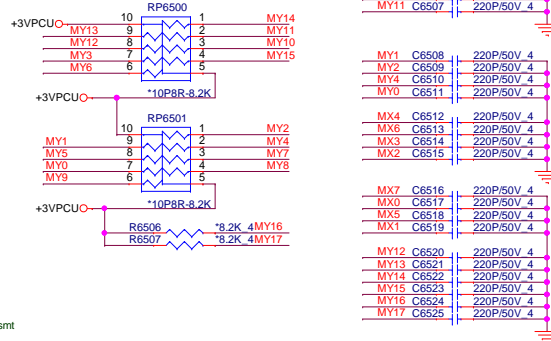


## USB/Phone Jack Connector

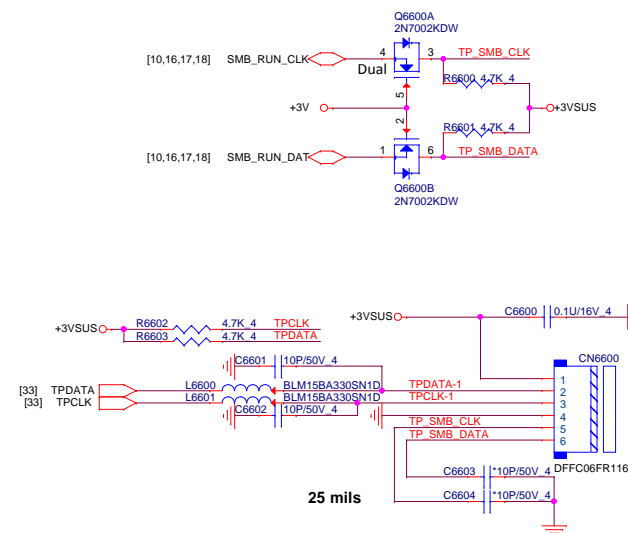




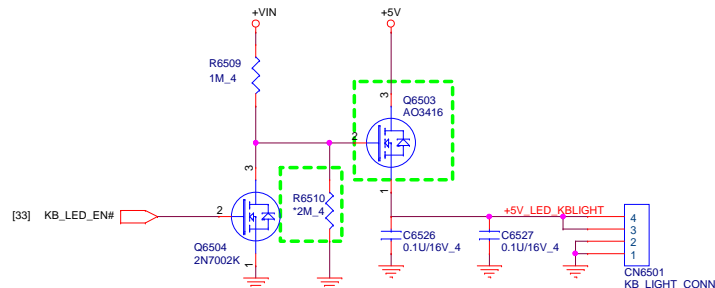
## KEYBOARD PULL-UP



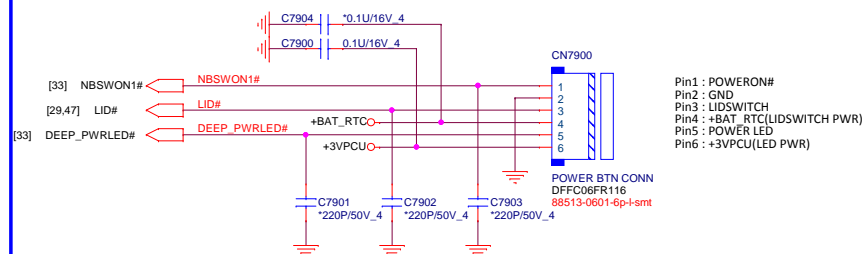
## Touch Pad Connector



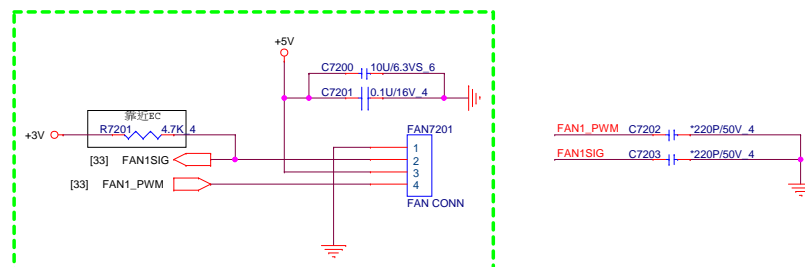
***KB LIGHT CONN***



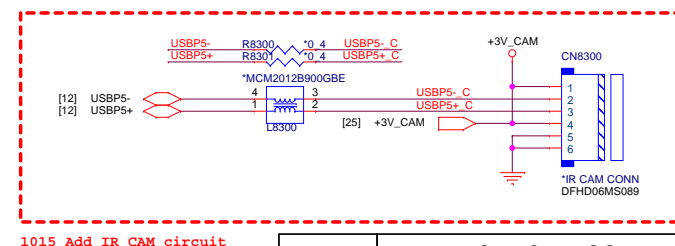
## Power Botton Connector



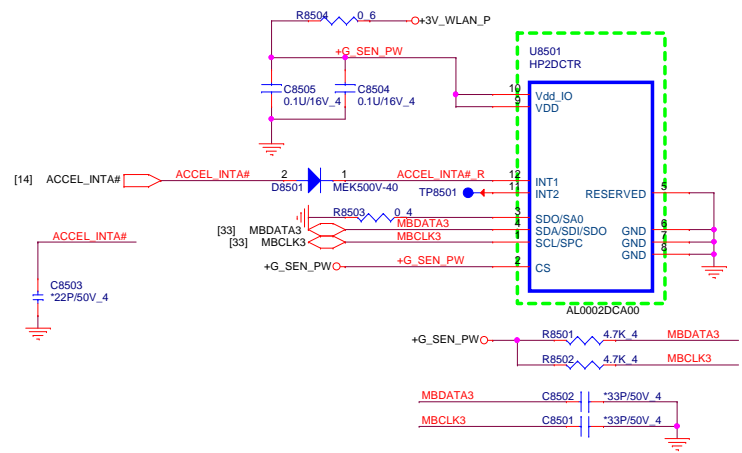
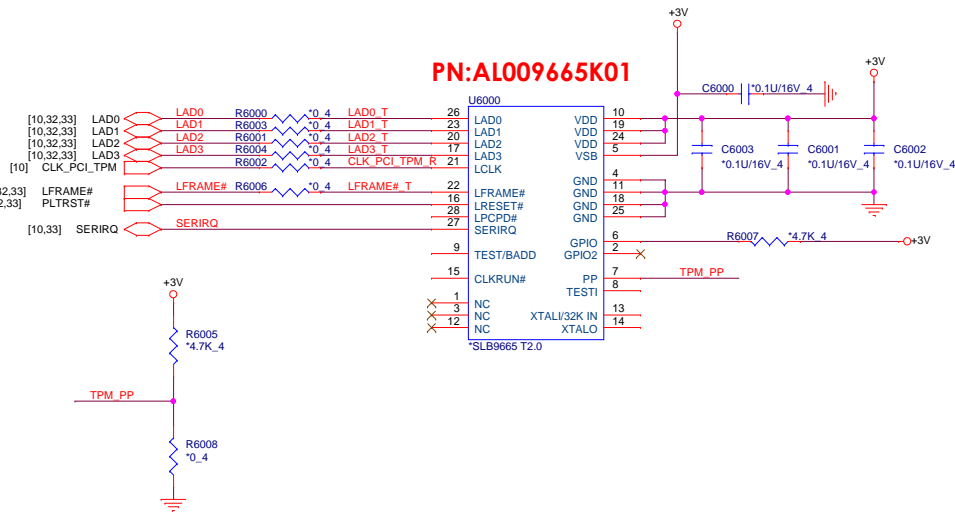
**FAN CONN**



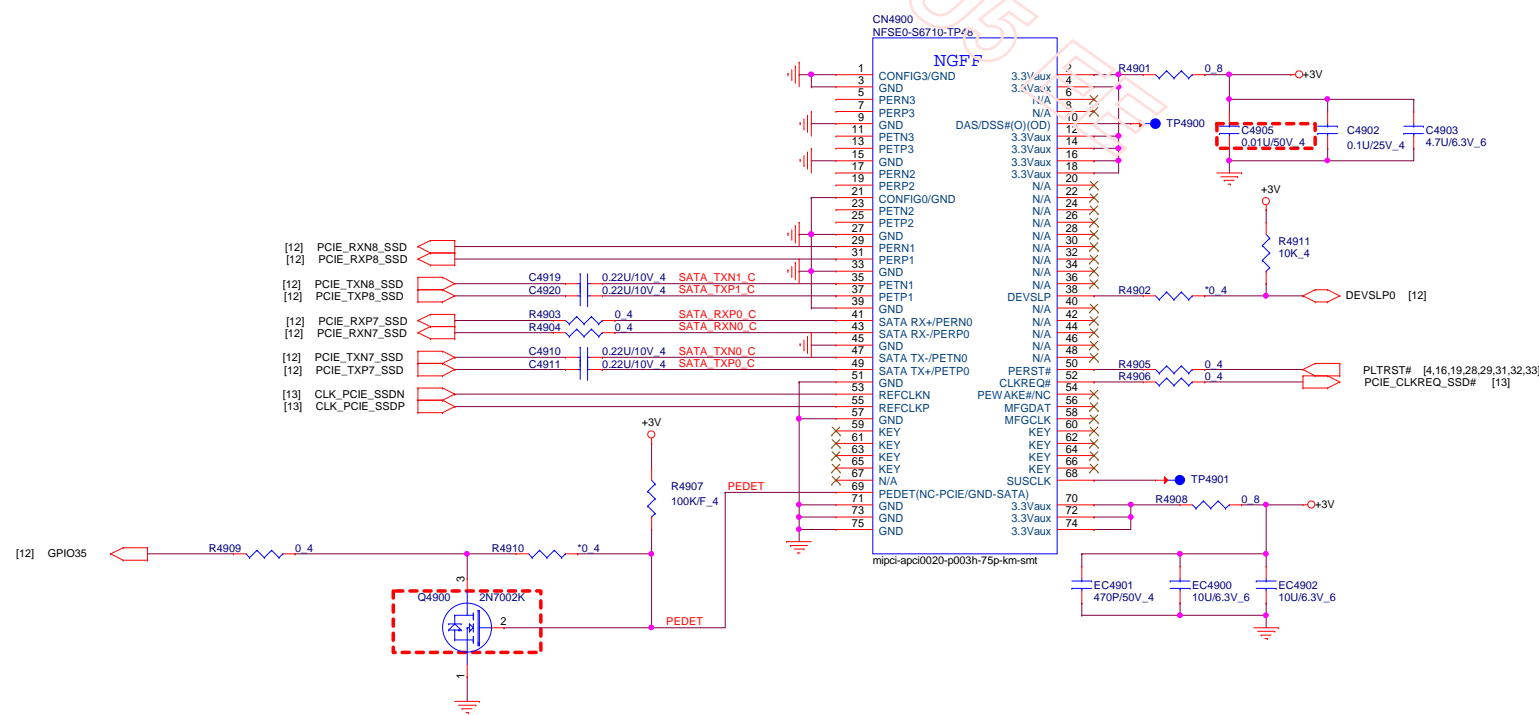
## IR CAM



## Accelerometer Sensor



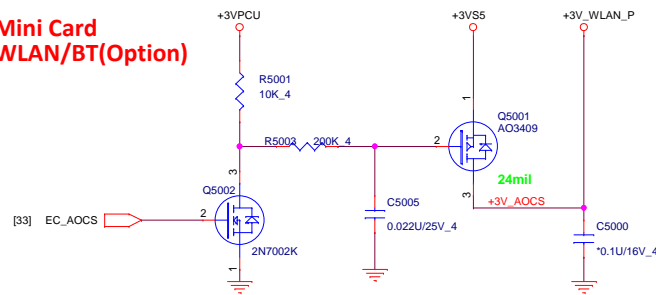
## SSD



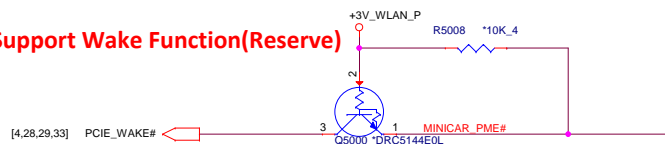
**PROJECT : G34A**  
Quanta Computer Inc.

Size Custom	Document Number <b>&lt;Doc&gt;</b>	Rev 1A
Date: Tuesday, January 05, 2016		Sheet 31 of 47

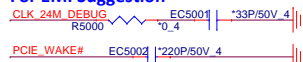
**Mini Card  
WLAN/BT(Optional)**



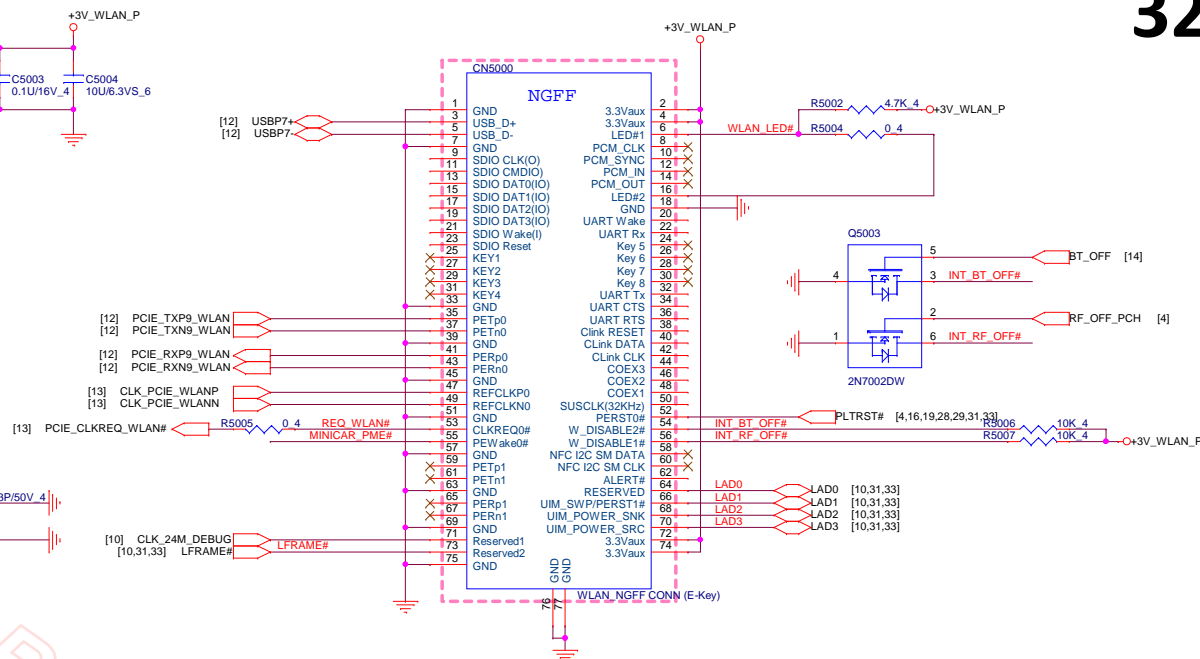
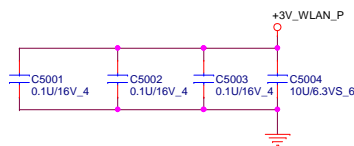
### Support Wake Function(Reserve)



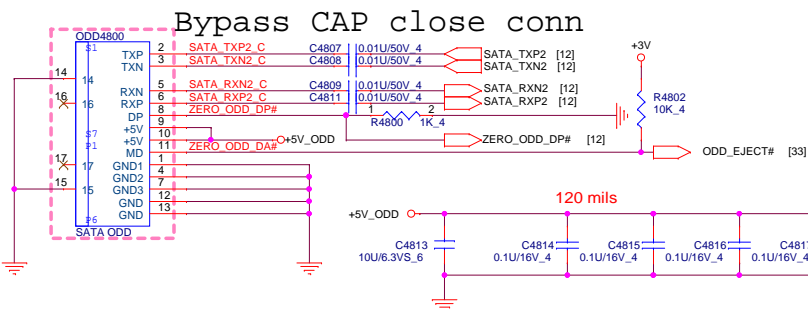
### For EMI Suggestion



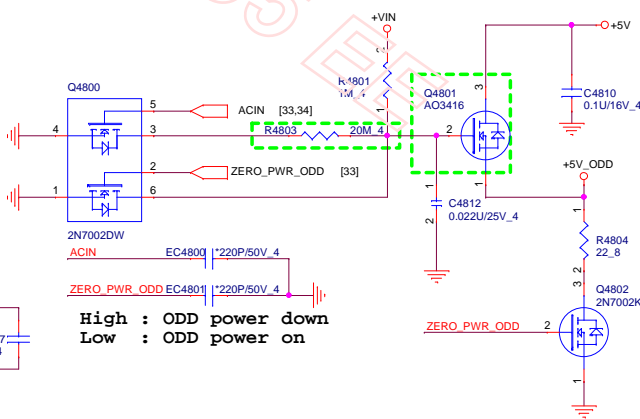
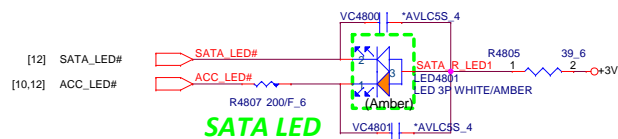
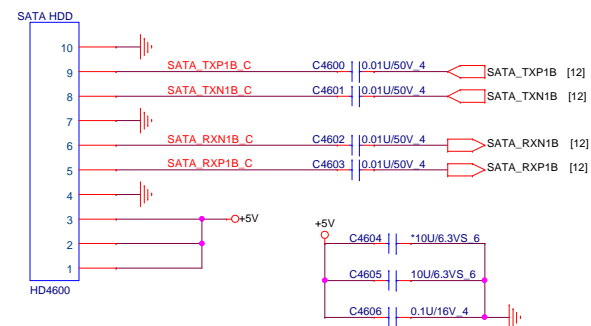
1020 del EC\_PCIE\_WAKE# circuit



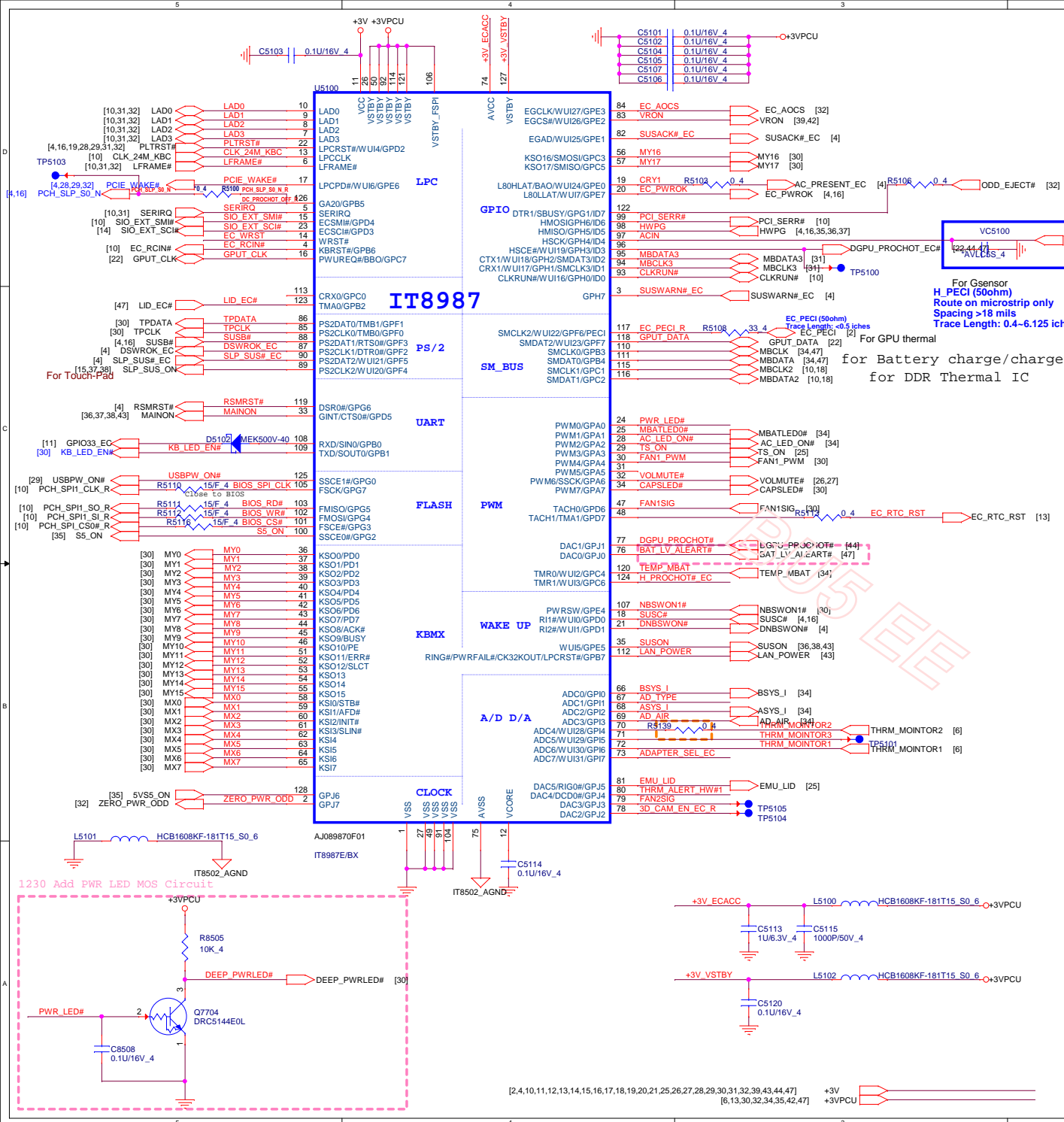
## SATA ODD



```
High : ODD power down
Low  : ODD power on
```

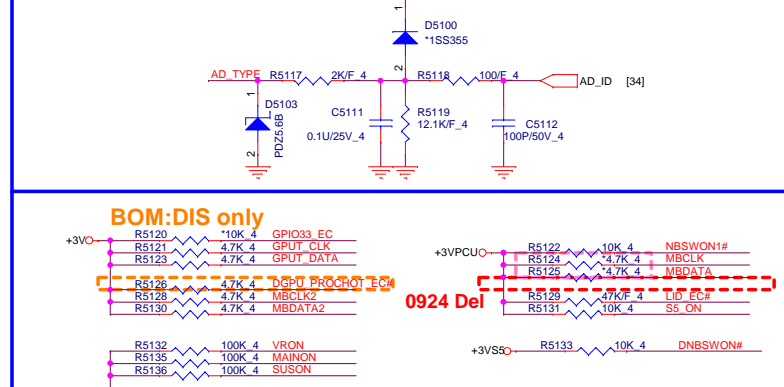
**HDD**

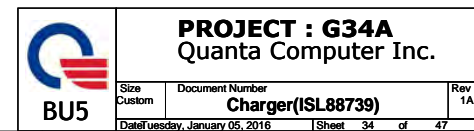




3VPCU  $\xrightarrow{R_{5114}}$  10K 4  $\xrightarrow{ADAPTER\_SEL\_EC}$  R5115  $\xrightarrow{2.2K\ 4}$  GND

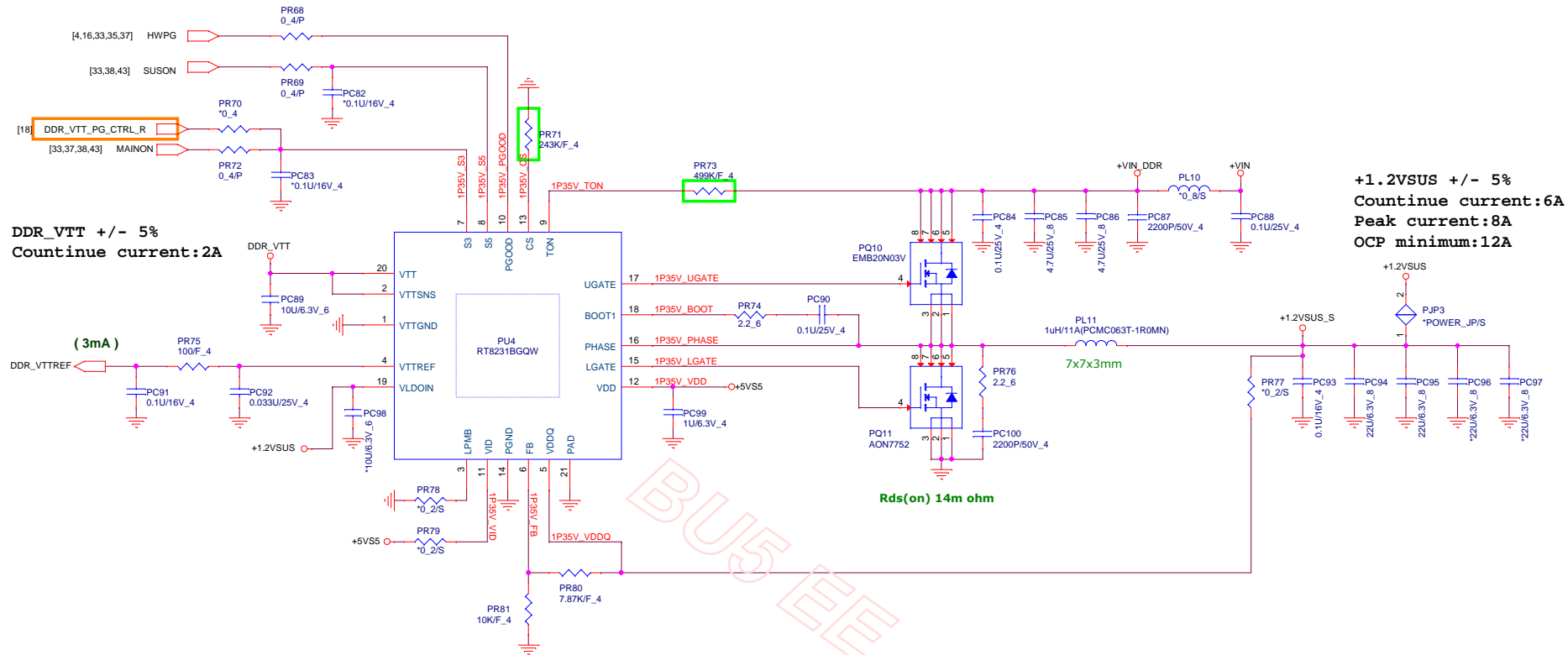
Labels: Ra, Rb



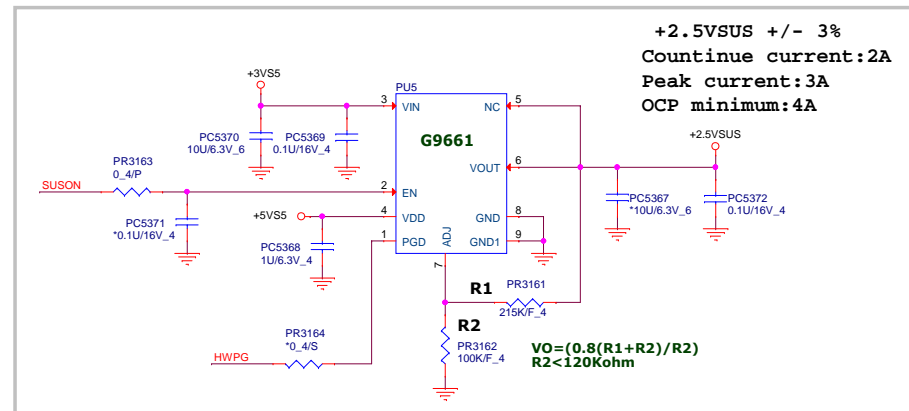




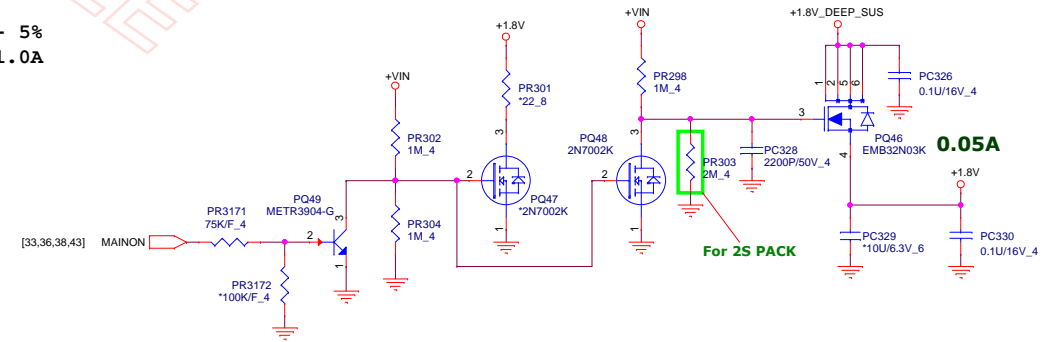
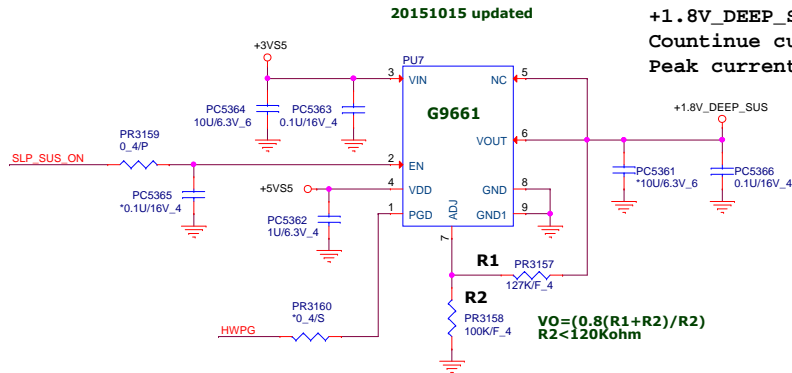
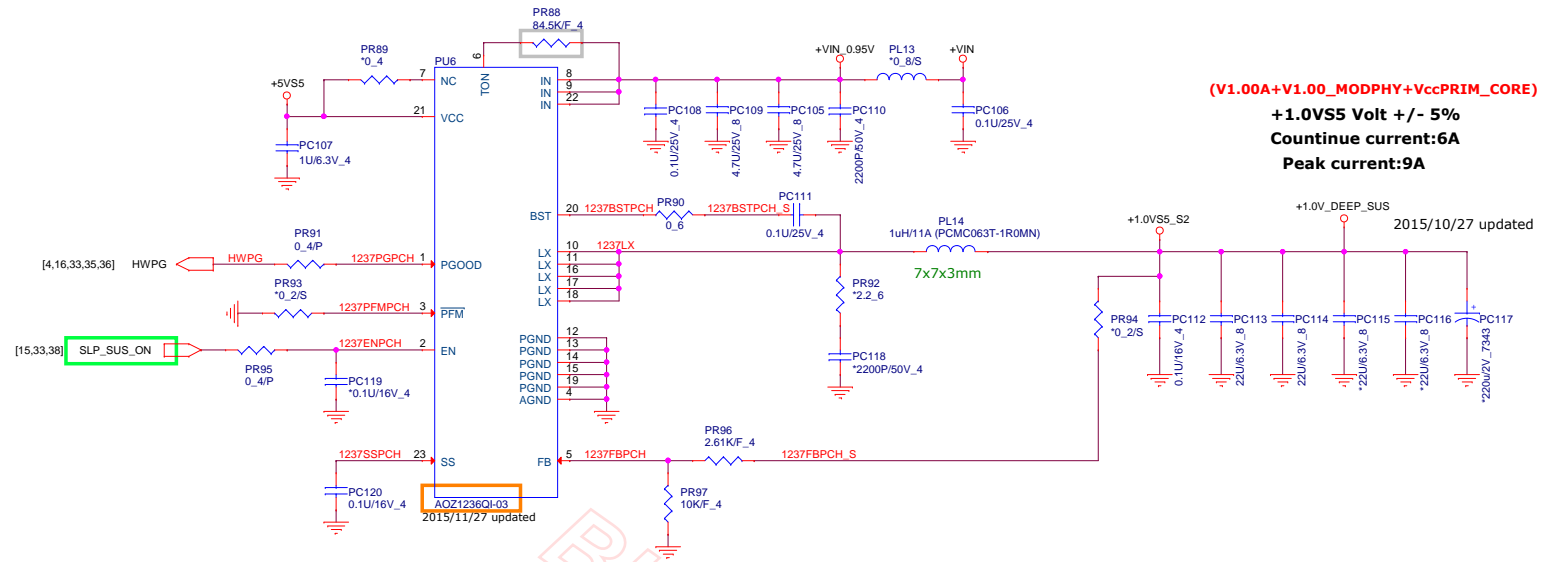
+VIN [25,30,32,34,35,37,39,40,41,42,44,45,47]  
 +5VS5 [4,25,26,29,35,37,38,39,40,41,43,44,45,46]  
 +1.2VSUS [3,6,17,18,38,46]  
 DDR\_VTT [17,18]



20151015 updated



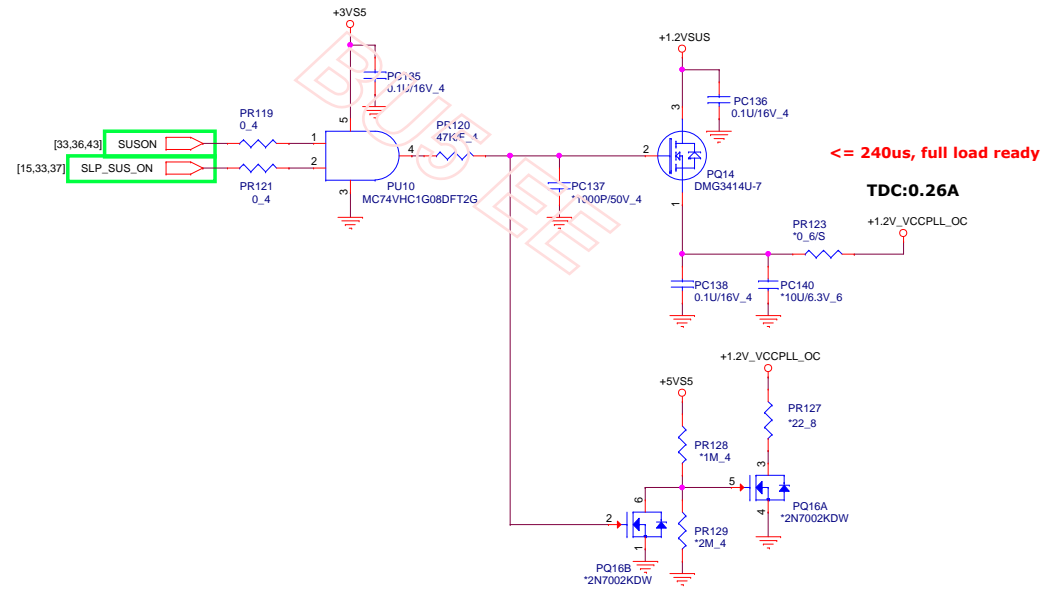
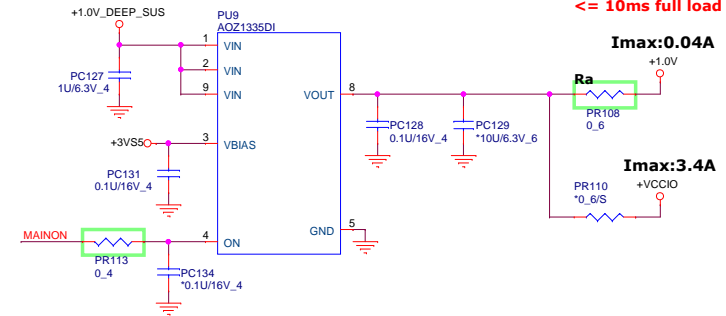
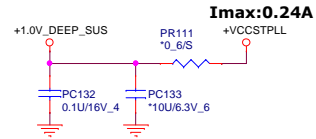
+VIN [25,30,32,34,35,36,39,40,41,42,44,45,47]  
 +3VS5 [4,10,15,16,25,32,33,35,36,38,42,43,46,47]  
 +5VS5 [4,25,26,29,35,36,38,39,40,41,43,44,45,46]  
 +1.0V\_DEEP\_SUS [9,13,15,16,38]  
 +1.8V\_DEEP\_SUS [5,9,15,47]  
 +1.8V [26]



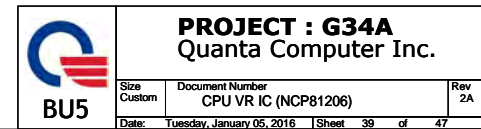
+1.0V [2,4,6,16,33]  
 +3VS5 [4,10,15,16,25,32,33,35,36,37,42,43,46,47]  
 +5VS5 [4,25,26,29,35,36,37,39,40,41,43,44,45,46]  
 +VCCIO [2,6,16]  
 +1.2VSUS [3,6,17,18,36,46]  
 +VCCSTPLL [2,4,5,6,9,39]  
 +1.0V\_DEEP\_SUS [9,13,15,16,37]  
 +1.2V\_VCCPLL\_OC [6]  
 MAINON [33,36,37,43]

**Volume Segment**  
**Vcc\_ST: 0.12A**  
**Vcc\_PLL: 0.12A**

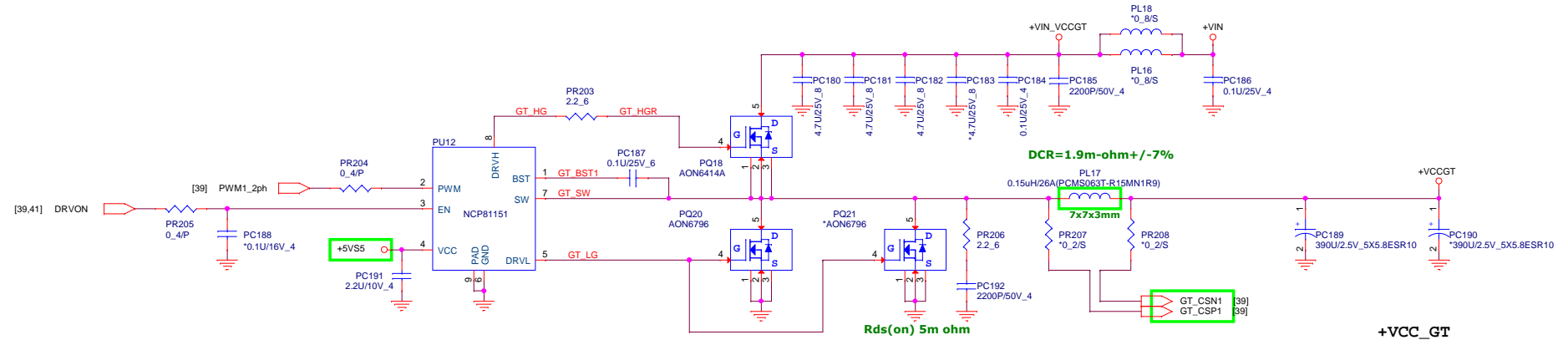
<= 10ms, full load ready  
 (Vcc\_ST+Vcc\_PLL)







+5V [25,26,27,30,32,43]  
 +VIN [25,30,32,34,35,36,37,39,41,42,44,45,47]  
 +5VPCU [26,34,35,43,46]  
 +VCCGT [7,39]



+VCC\_GT

U-line 22 (15W)

TDC: 18A(22)

Icc max: 31A(22)

L/L=3.1mV/A

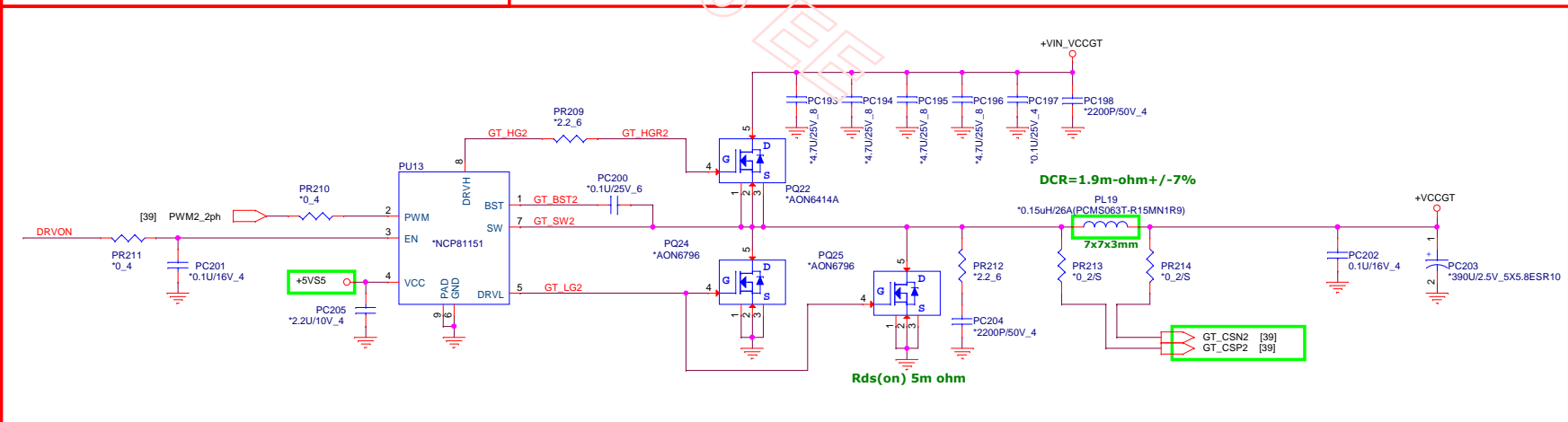
U-line 23e(28W)

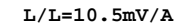
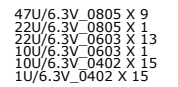
TDC: 35A(23e)

Icc max =64A(GT+GTx)

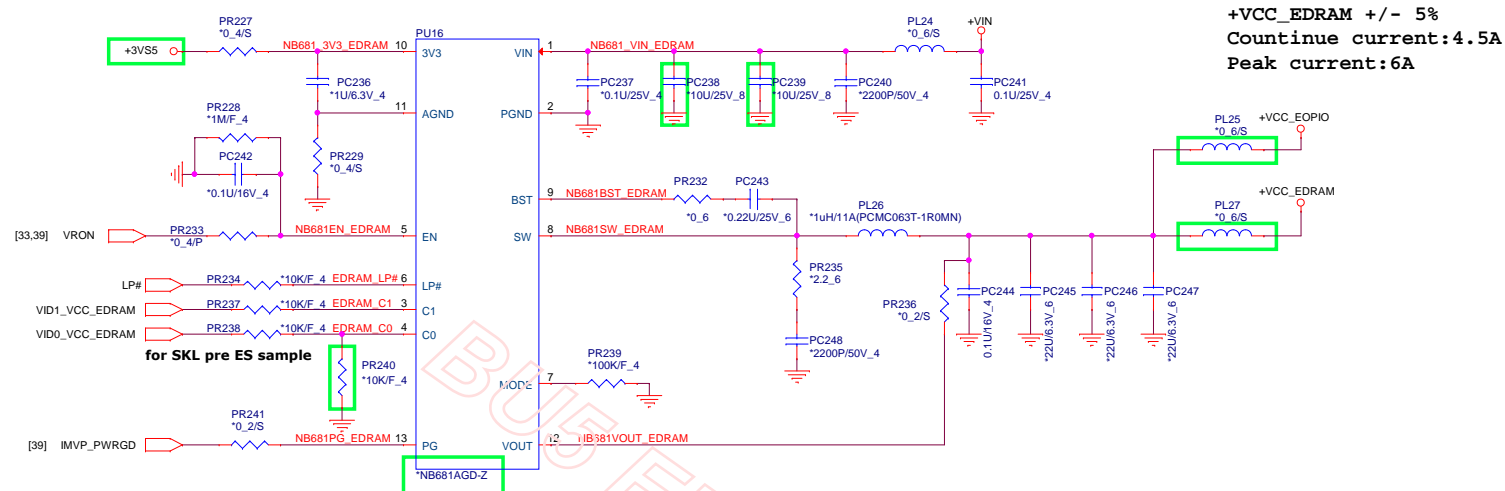
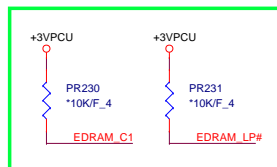
L/L=2mV/A

For U23e --> Add These Components





+VIN [25,30,32,34,35,36,37,39,40,41,44,45,47]  
 +3VPCU [6,13,30,32,33,34,35,47]  
 +VCC\_EOPIO [5]  
 +VCC\_EDRAM [5]



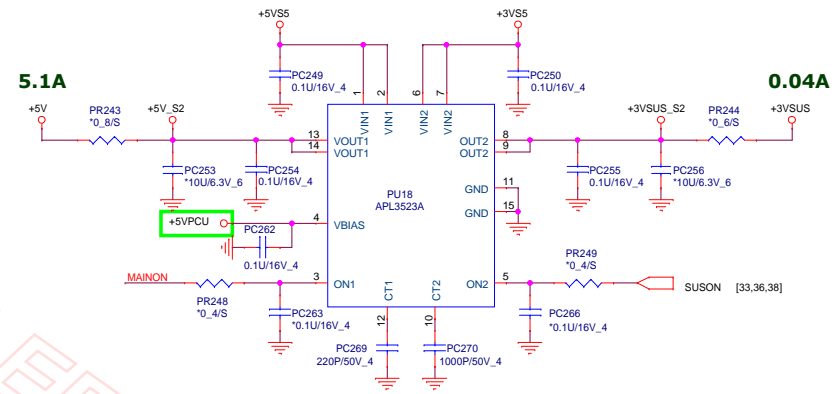
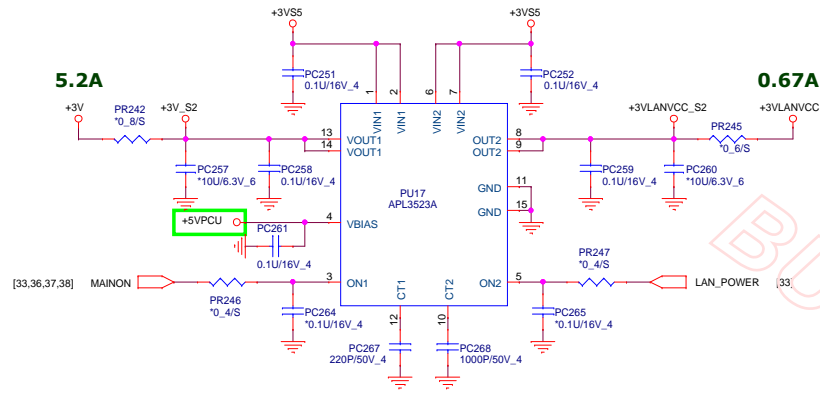
#### VCC\_EDRAM

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

#### MODE

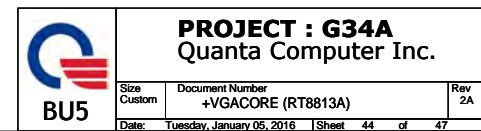
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

+3V	[2,4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,44,47]
+5V	[25,26,27,30,32]
+VIN	[25,30,32,34,35,36,37,39,40,41,42,44,45,47]
+3VS5	[4,10,15,16,25,32,33,35,36,37,38,42,46,47]
+5VS5	[4,25,26,29,35,36,37,38,39,40,41,44,45,46]
+3VSUS	[30]
+5V_CAM	
+3VLAVCC	[28]

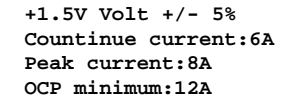


**PROJECT : G34A**  
**Quanta Computer Inc.**

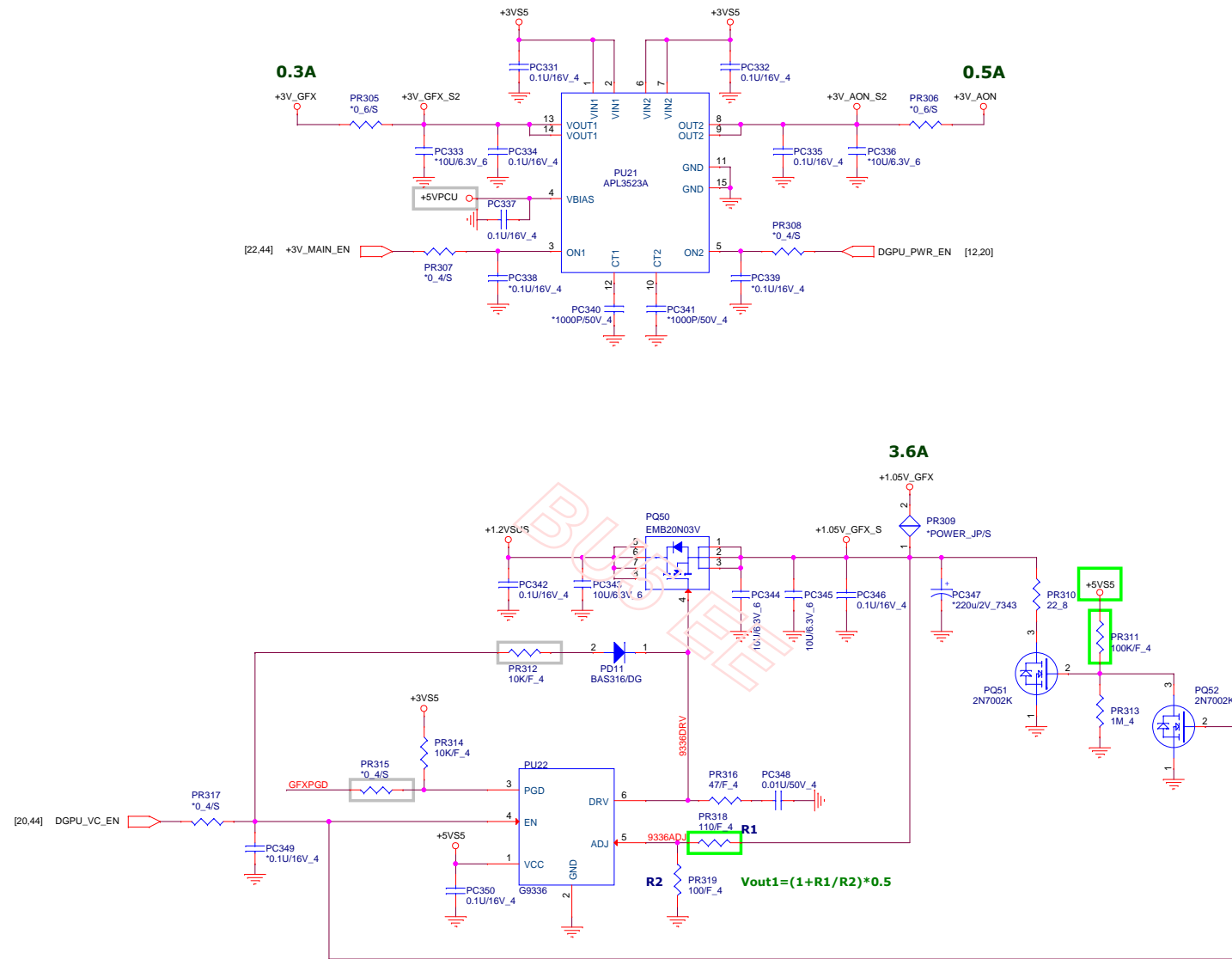
Size Custom	Document Number <b>Dis-charge IC (SLG55448)</b>	Rev 1A
Date: Tuesday, January 05, 2016	Sheet 43 of 47	

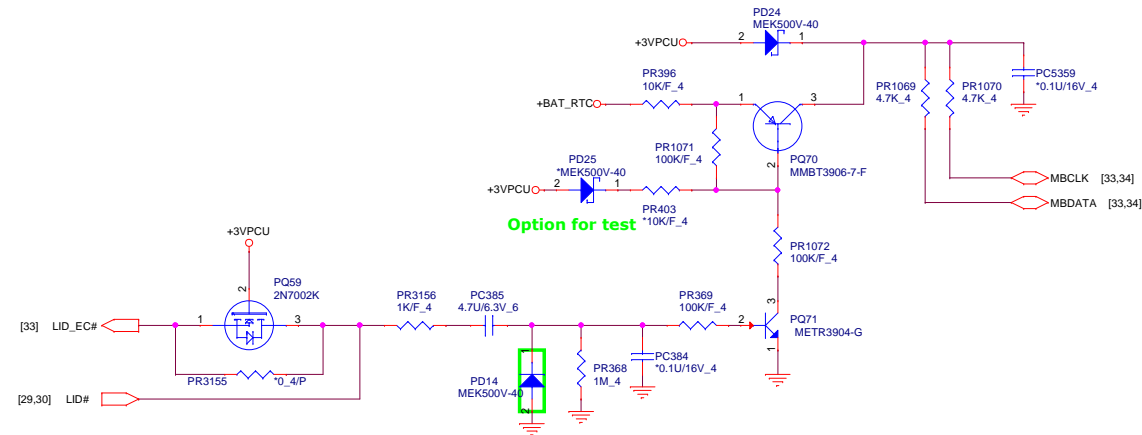






+VIN [25,30,32,34,35,36,37,39,40,41,42,44,45,47]  
 +3VS5 [4,10,15,16,25,32,33,35,36,37,38,42,43,47]  
 +5VS5 [4,25,26,29,35,36,37,38,39,40,41,43,44,45]  
 +3V\_GFX [19,21,22,44,45]  
 +3V\_AON [19,22]  
 +1.2VSUS [3,6,17,18,36,38]  
 +1.05V\_GFX [19,20,21]





20160105 updated

